CIRCUIT ANALYSIS REPORT

Manufacturer Part No.

—— DDR

Science Vision

Visualized Fact Utmost Science

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PART A

Project Overview

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1.0 Project Introduction

1.1 Chip Introduction

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Application:
- XXXXXXXXXXXXXXXXXXXXXX
- XXXXXXXXXXX
- XXXXXXXXXXXXXXXXXX

1.2 Device Summary

Item	Content
Part Number / Project Number	XXXXXXXX / XXXXXXX
Manufacturer	XXXXXXX
Device Type	XXXXXXXXXXXXXXXX
Package Marking	XXXXXXXXXX; XXXXXX; XXXXXXXXXX;
Package Type	XXXXXXXXX
Die Marking	XXXXXXX; XXXX; XXXXXXXXX;
Die Size	9.04 mm × 5.40 mm = 48.816 mm^2
Number of Metal Layers	3
Number of Poly Layers	1
Process Type	CMOS
Interconnect Level (Width/Pitch(nm))	
Process Generation	XX nm
Feature Measure to Determine Process Generation	Gate Length
Transistor Gate Length	XX nm

2.0 Device Identification

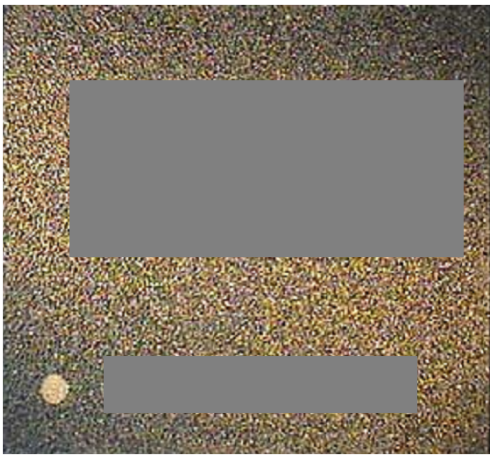
This section contains information regarding the packaging, die marking and die photo of Manufacurer Part No.

Section 2.1 contains the package photo.
Section 2.2 provides die photo.
Section 2.3 provides X-ray photo.

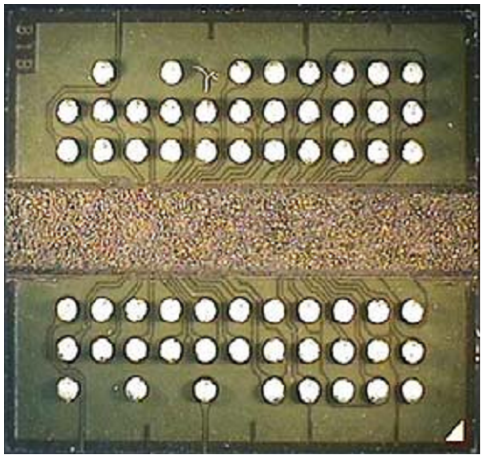
2.1 Package Photo

This Manufacurer Part No is packaged inside a 60-pin XXXX Package.

Photographs of the top and bottom view of the packages are shown in Photograph 2.1.1 and 2.1.2. Photograph 2.1.3. is an x-ray photograph of the device presenting external pins.

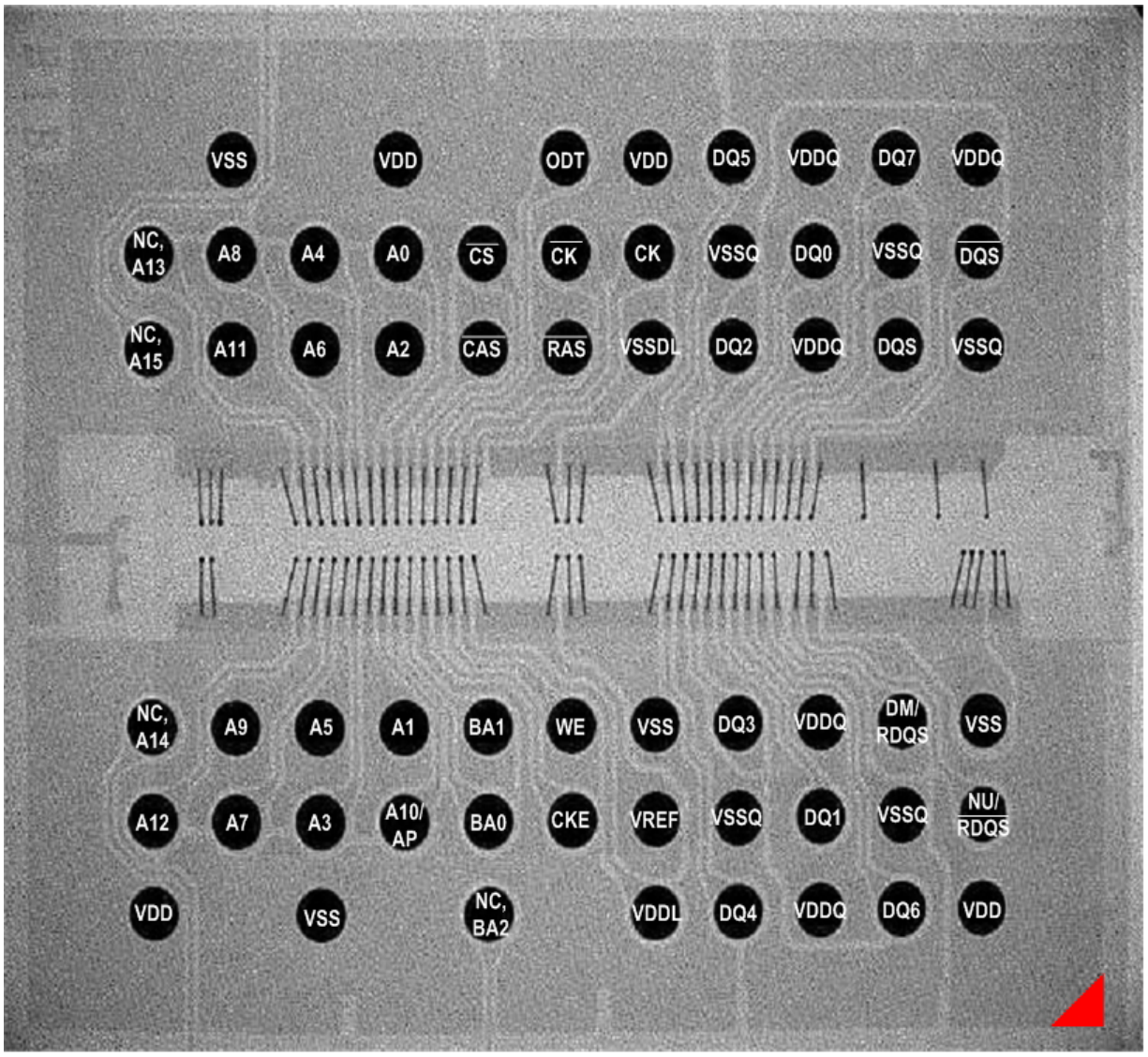


Photograph 2.1.1 Package (top)



Photograph 2.1.2 Package (bottom)

2.2 X-ray Photo



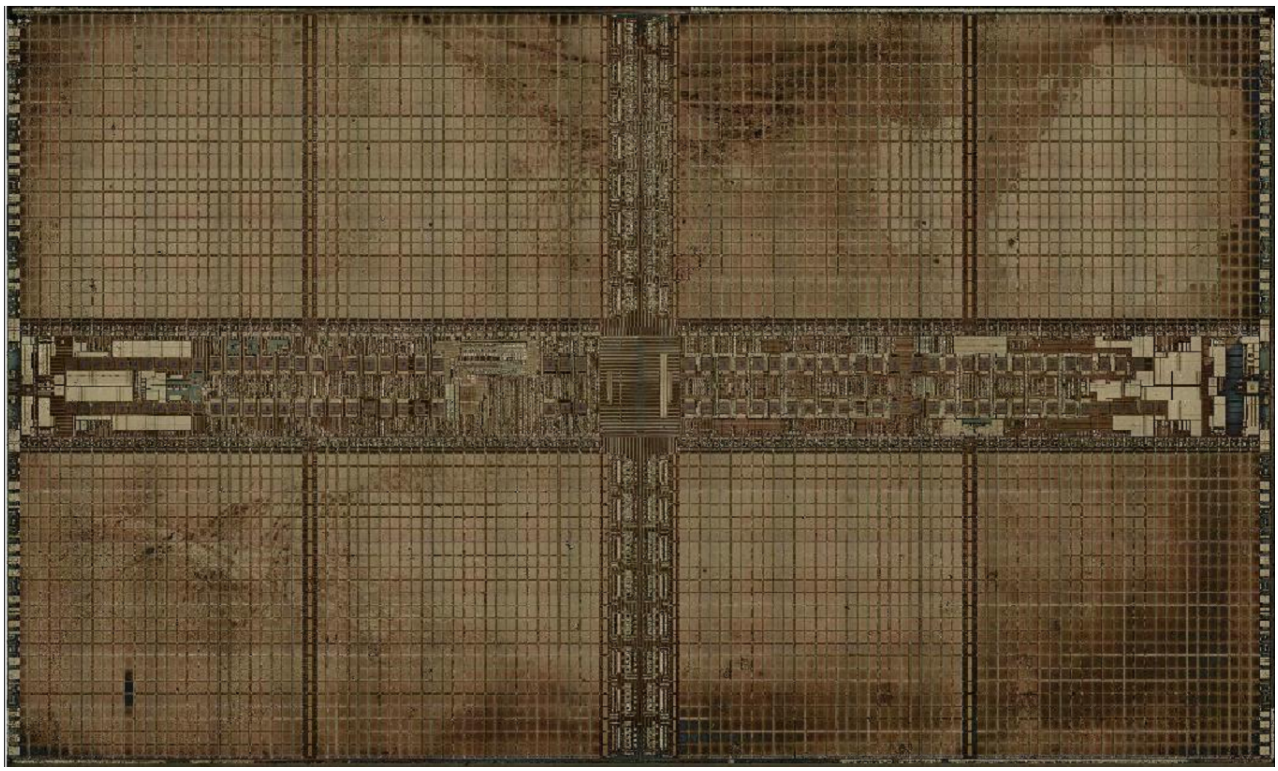
Pin 1 Indication

Photograph 2.1.3 X-ray

2.2 Die Photo

Manufacurer Part No is produced using a 3 metal, one poly XX nm CMOS process.

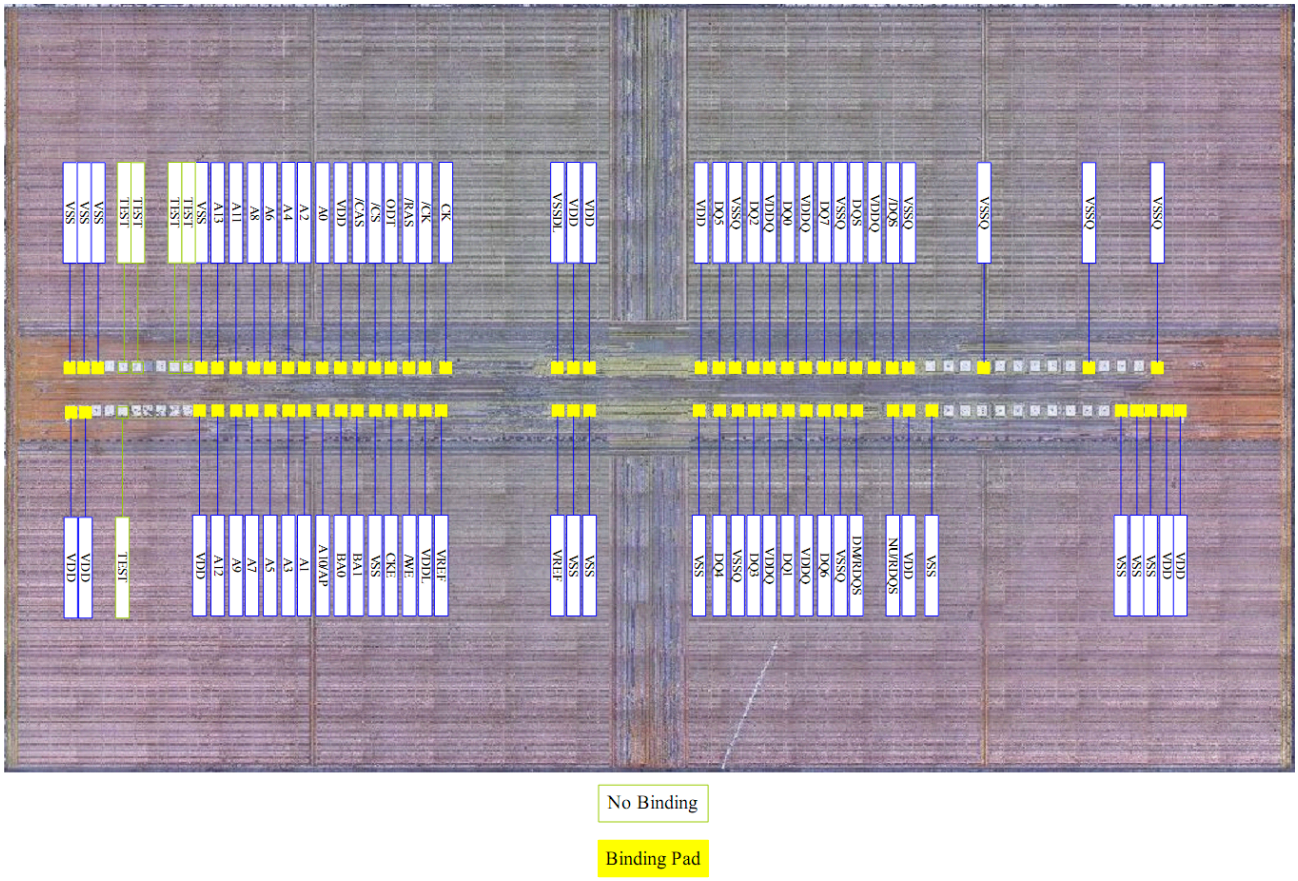
The die measures 48.816 mm^2 =9.04 mm × 5.40 mm and is presented in Photograph 2.2.



Photograph 2.2 Die Photo (Poly Stained Image)

2.3 Pad Definition

The pad layout of the device is illustrated in Photograph 2.3.



Photograph 2.3 Die Photo (Metal-3 Image)

2.4 Die Marking

The die marking is presented in Photograph 2.4.

Photograph 2.4 Die Marking

3.0 Parameter Definition

The following standards for parameter definition are used in this report:

The measurements of MOS transistor are expressed as:

W*M/L*N

Where W= gate width of MOS transistor

L= gate length of MOS transistor

M= number of transistors connected in parallel

N= number of transistor connected in series

(When M=1 and N=1, the parameter of MOS transistor is expressed simply as W/L)

The measurements of Bipolar Junction Transistor are expressed as:

Se=area of emitter region for one BJT

Pe= perimeter of emitter region for one BJT

M= number of the BJTs connected in parallel

For diode, the parameter is expressed as:

S= area of heavily doped region for one diode

M= number of diodes connected in parallel

For capacitor, the parameter is expressed as:

W*M/L

Where W= width of one capacitor

L= length of one capacitor

M= number of capacitors connected in parallel

The measurements of finger capacitor are expressed as:

W= width of one finger

L= length of one finger

Space=space between fingers

M= number of finger capacitors in parallel

Layers= metal layers used for the finger capacitor

Type= VPP for parallel plate and VSP for staggered plate

The measurements of resistor are expressed as:

W=Xμm and L= Xμm, where W=width, L= length

For the resistors connected in series, the measurements are expressed as:

W= X and L=X*N, where W=width, L= length and N is the number of resistors connected in series.

For the resistors connected in parallel, the measurements are expressed as:

W= X*M and L=X, where W=width, L= length and M is the number of resistors connected in parallel.

For digital instance, the parameter is expressed as:

WP*MP/LP
WN*MN/LN

WP= gate width of PMOS transistor WN = gate width of NMOS transistor

LP = gate length of PMOS transistor LN = gate length of NMOS transistor

MP= number of PMOS transistors connected in parallel

MN= number of NMOS transistors connected in parallel

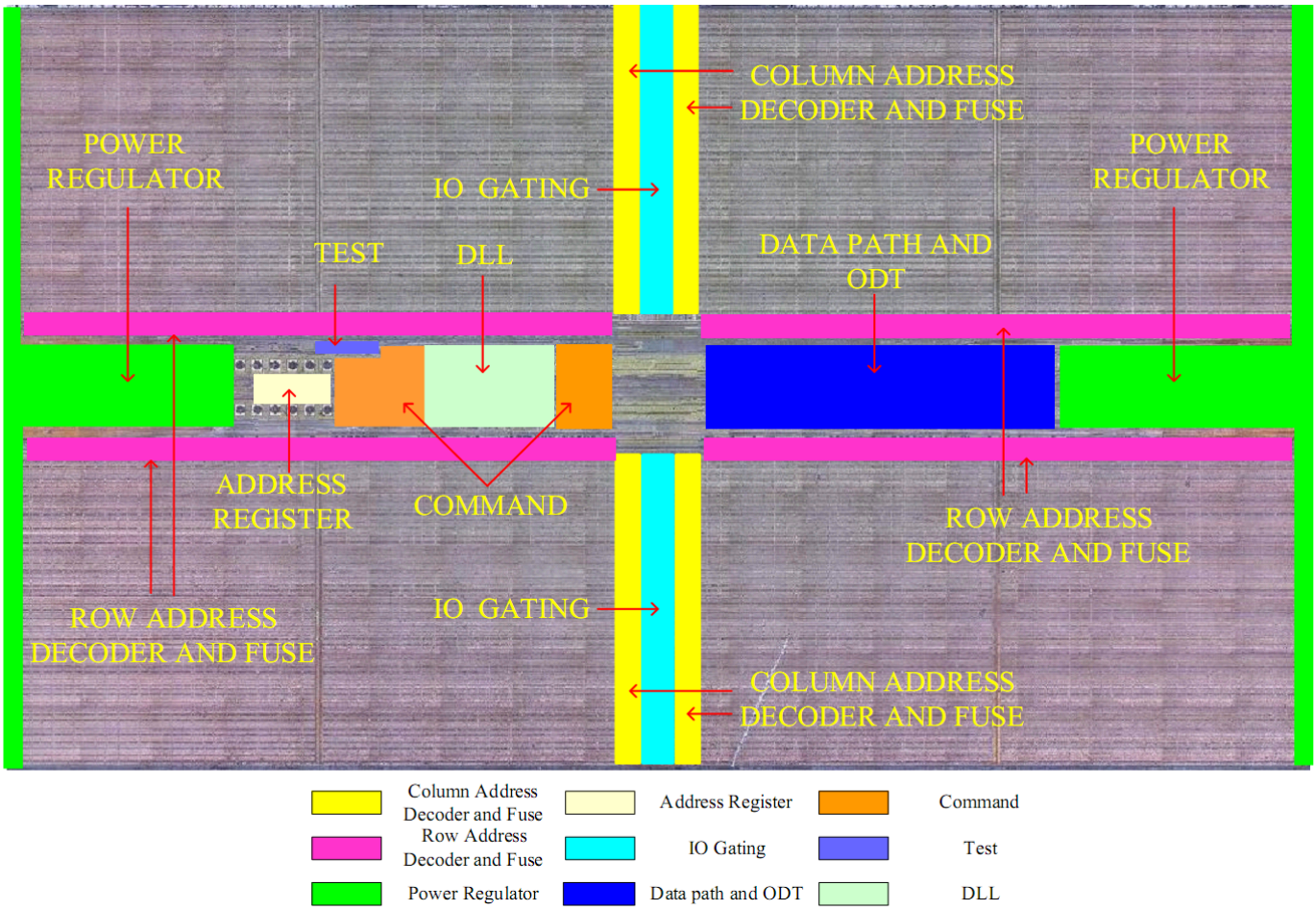
(When M=1, the parameter of digital instance is expressed simply as WP/LP, WN/LN)

4.0 Architecture & General Overview

This section includes the following functional information about the die:

- Die Architecture
- Block Diagram
- Address Architecture and Bitmap
- Power Map

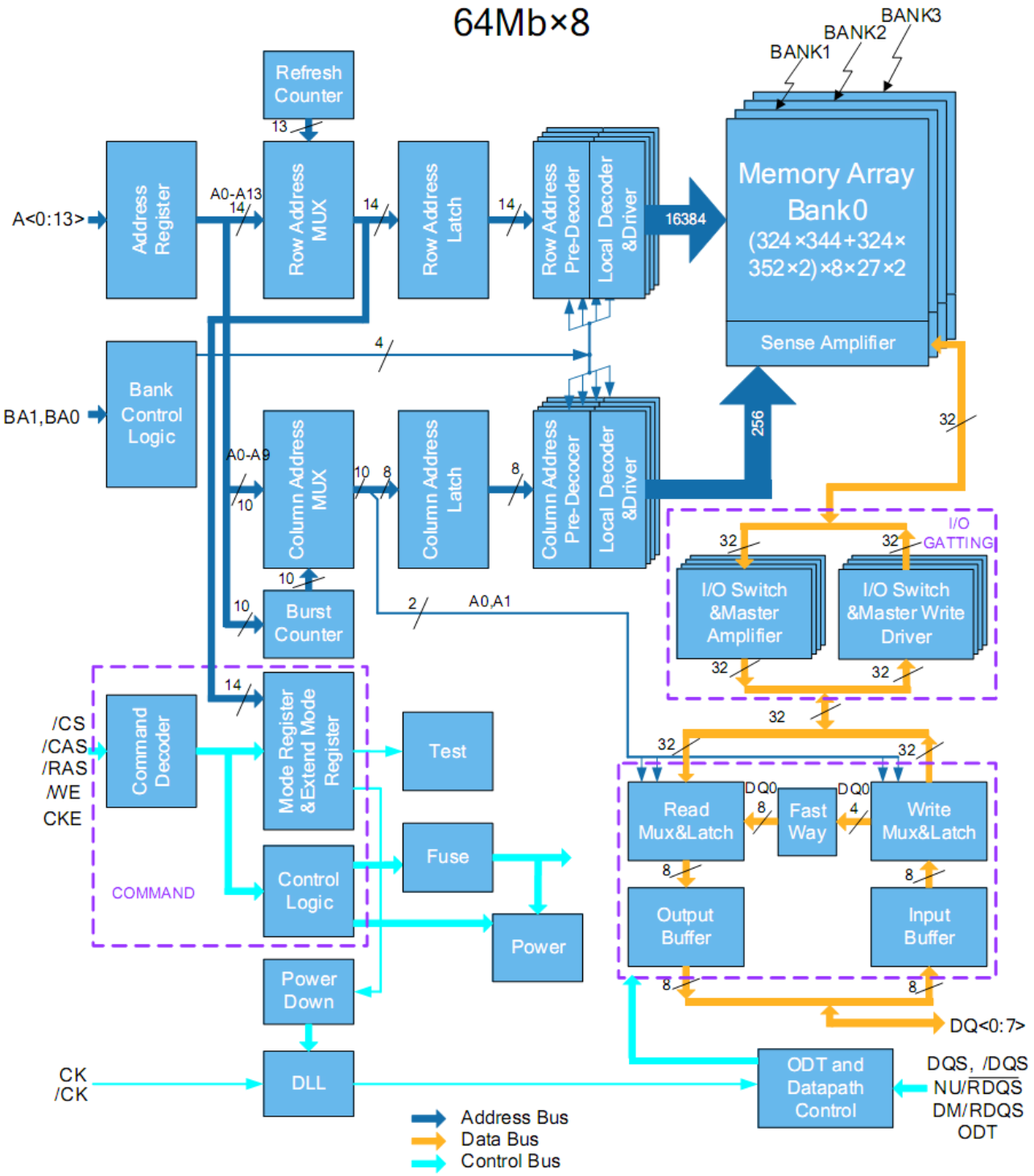
4.1 Die Architecture



Photograph 4.1 Die Architecture (M3 Image)

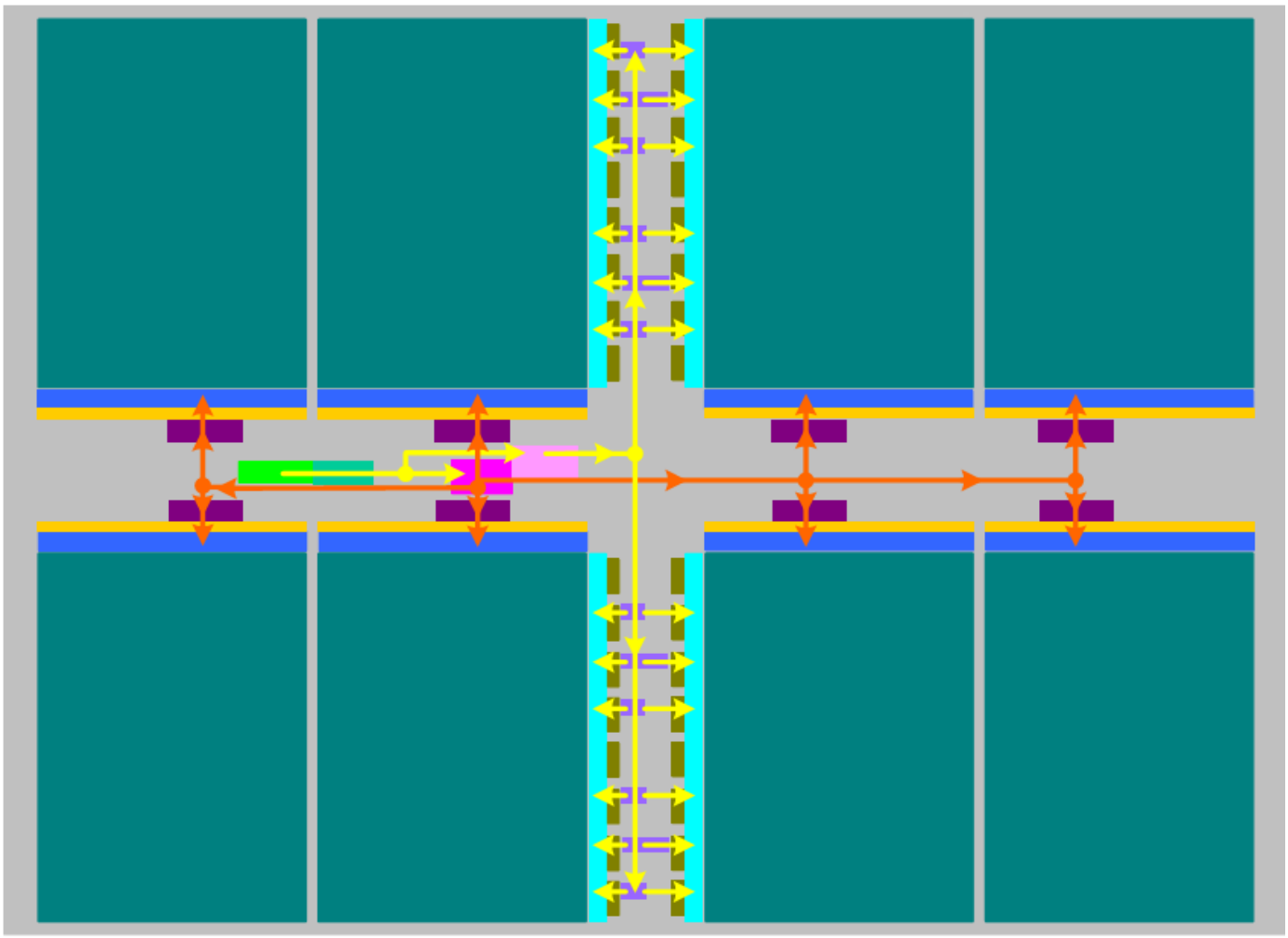
1. Each color block is presented a function block in Photograph 4.1.
2. The power supply blocks are mirrored in the left and right side of the chip (Green Block). They can supply power symmetrically to the whole chip.
3. The whole address path mainly includes ADDRESS REGISTER, ROW/COLUMN DECODER and FUSE.
4. The whole data path mainly contains DATAPATH, ODT AND I/O GATING.

4.2 Block Diagram



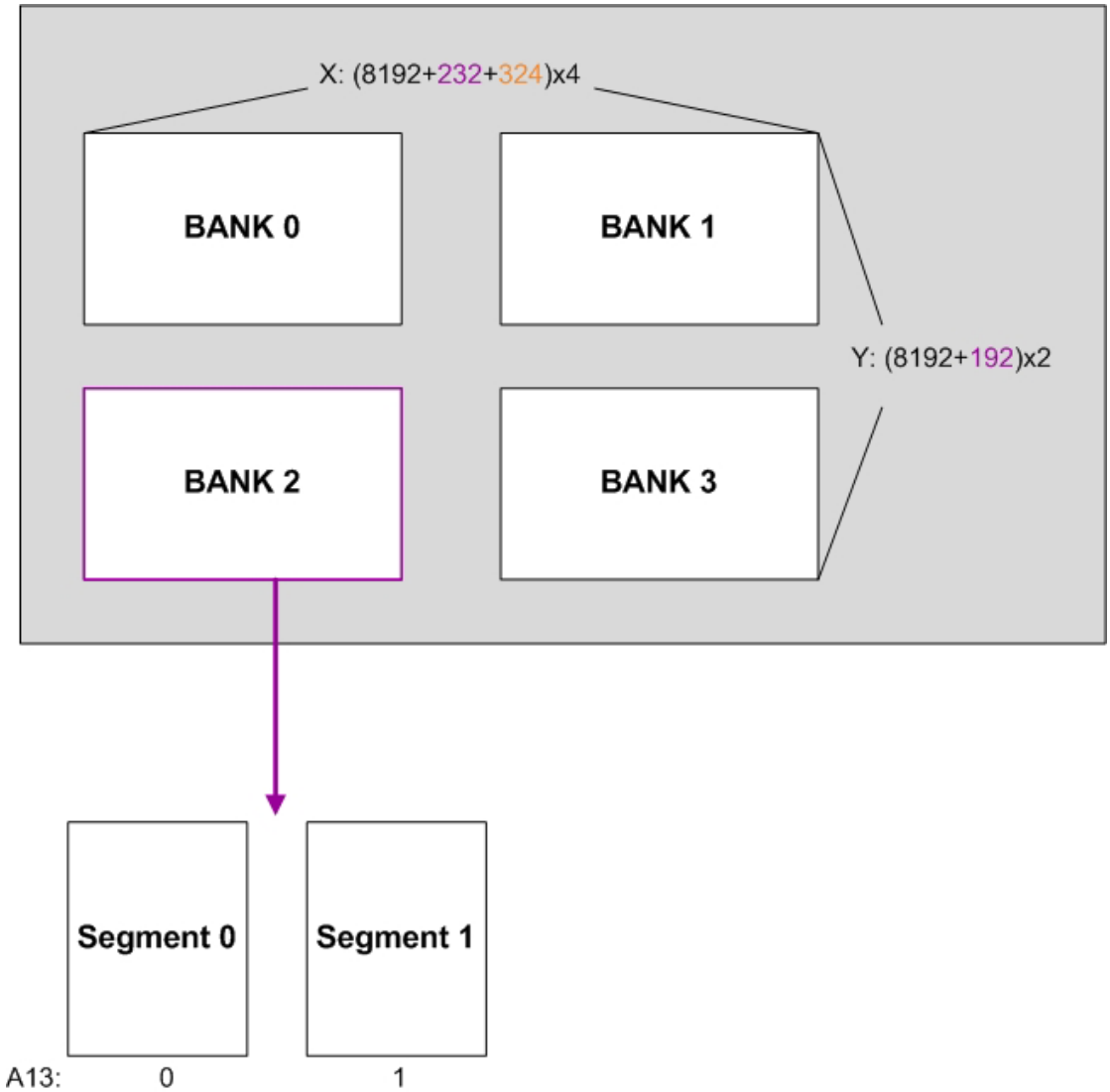
Photograph 4.2 Block Diagram

4.3 Address Architecture and Bitmap



Address Register (A0-A13)
BA Register (BA0,BA1)
Bank Select Decoder
Refresh Counter
Row Address Mux
Row Address Latch
Row Pre-Decoder
Row Decoder&Driver
Row Fuse
Burst Counter
Column Address Mux
Column Address Latch
Column Pre-Decoder
Column Decoder&Driver
Column Fuse

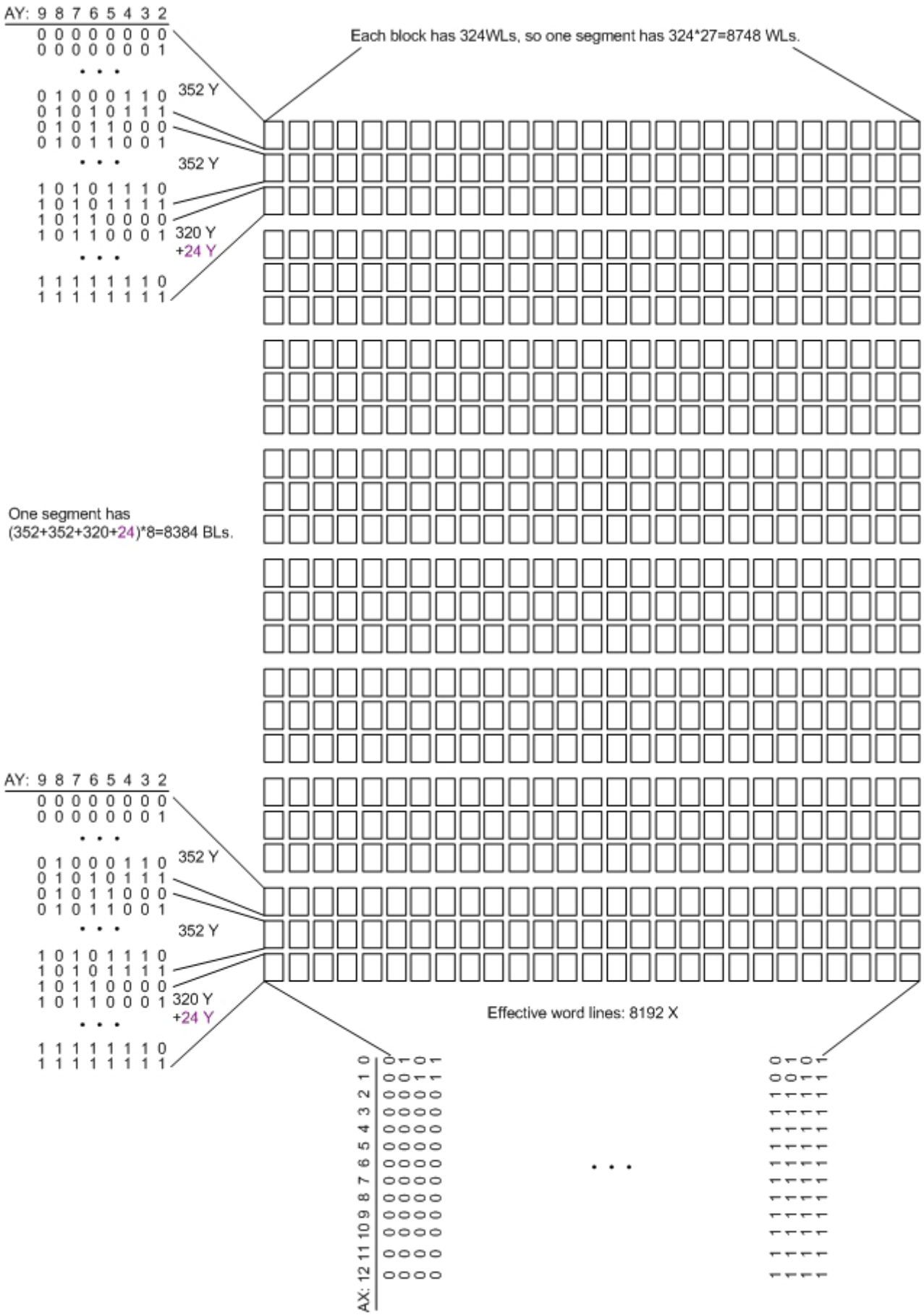
Photograph 4.3.1 Address Architecture



Photograph 4.3.2 Address Bitmap-Bank

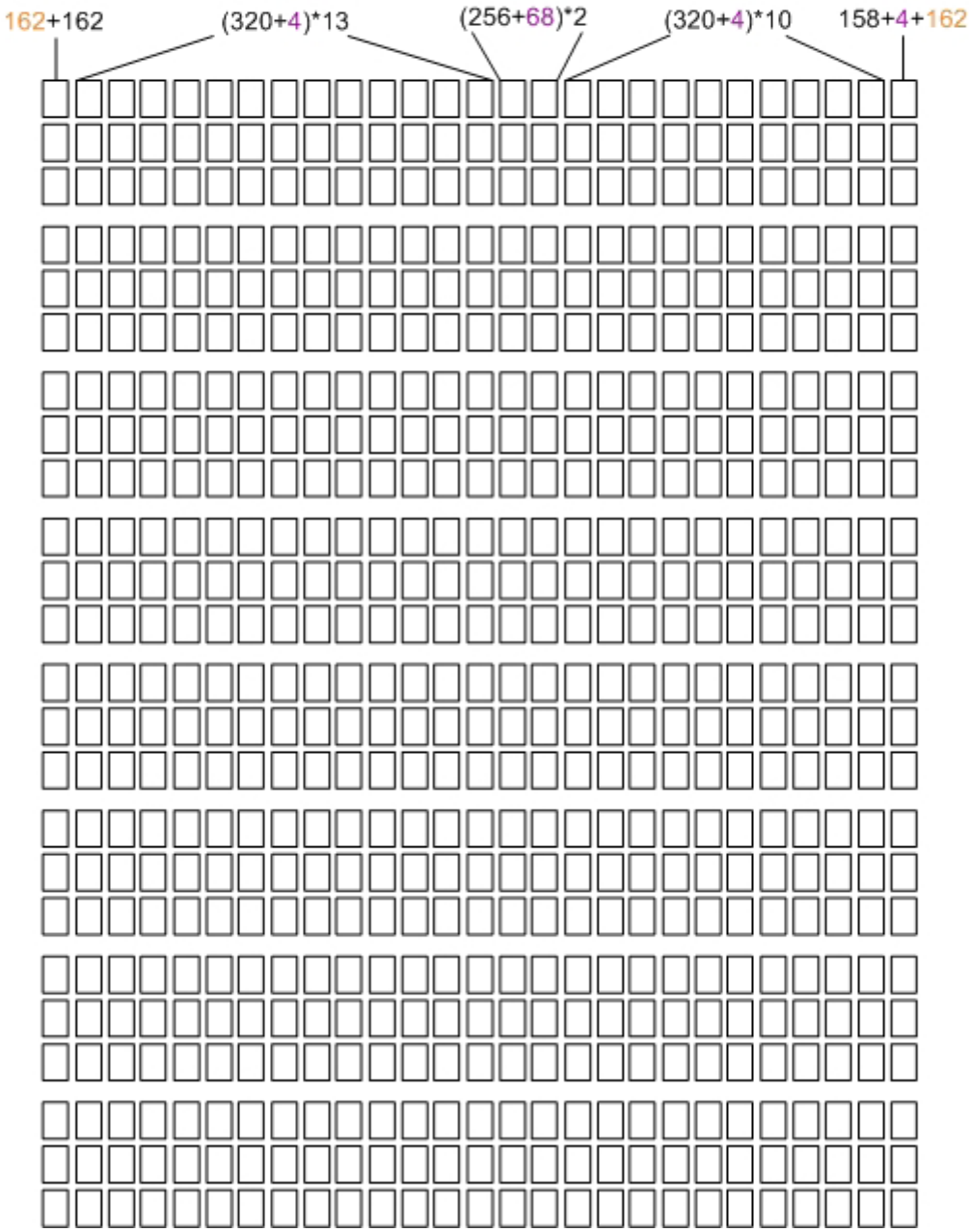
This chip has 33696(=8192x4+232x4) useful word lines, 1296(=324x4) dummy word lines and 16768(=8192x2+192x2) bit lines.
32768(=8192x4) word lines are effective, 928(=232x4) word lines are redundancy.
16384(=8192x2) bit lines are effective, 384(=192x2) bit lines are redundancy.

This memory total capacity: (8192+232+324) x 4 x (8192+192) x 2 = 586,745,856 bits.
This memory effective capacity: 32768 x 16384 = 536,870,912 bits = 512M bits.
This memory redundancy capacity: 928 x 16768 + 384 x 32768 = 28,143,616 bits.
This memory dummy capacity: 1296 x 16768 = 21,731,328 bits
The effectivity of the memory is 536,870,912/586,745,856 = 91.50%



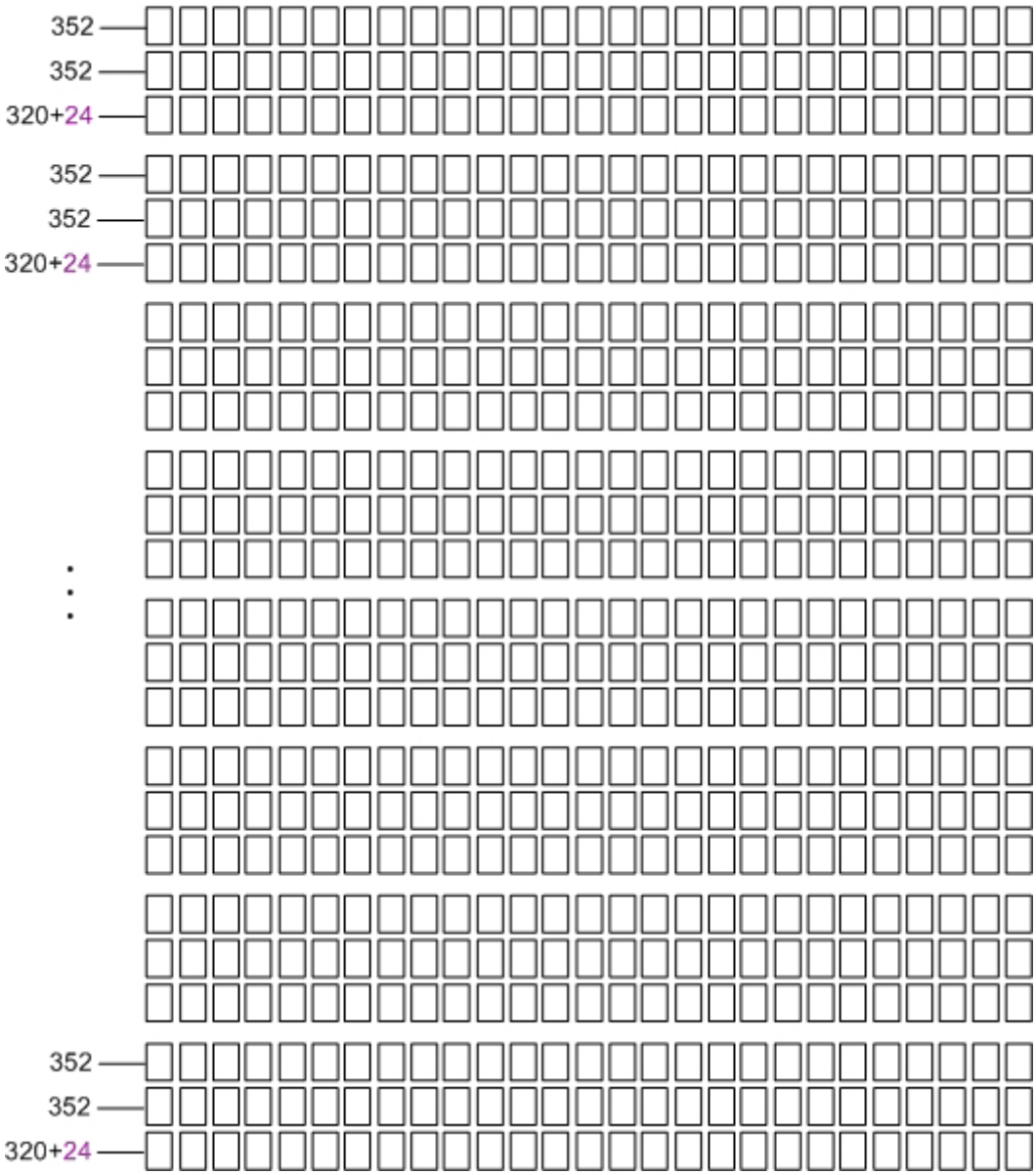
Photograph 4.3.3 Address Bitmap-Segment

Each block has 324WL, so one segment has 324*27=8748.
232+8192+324=8748
There are 232=4*13+68*2+4*10+4 redundant word lines in each segment.
There are 8192=162+320*13+256*2+320*10+158 effective word lines in each segment.
There are 324=162+162 dummy word lines in each segment.



Photograph 4.3.4 Row Redundancy Bitmap

There are 192=24*8 redundant word lines in each segment.
There are 8192=(352+352+320)*8 effective word lines in each segment.



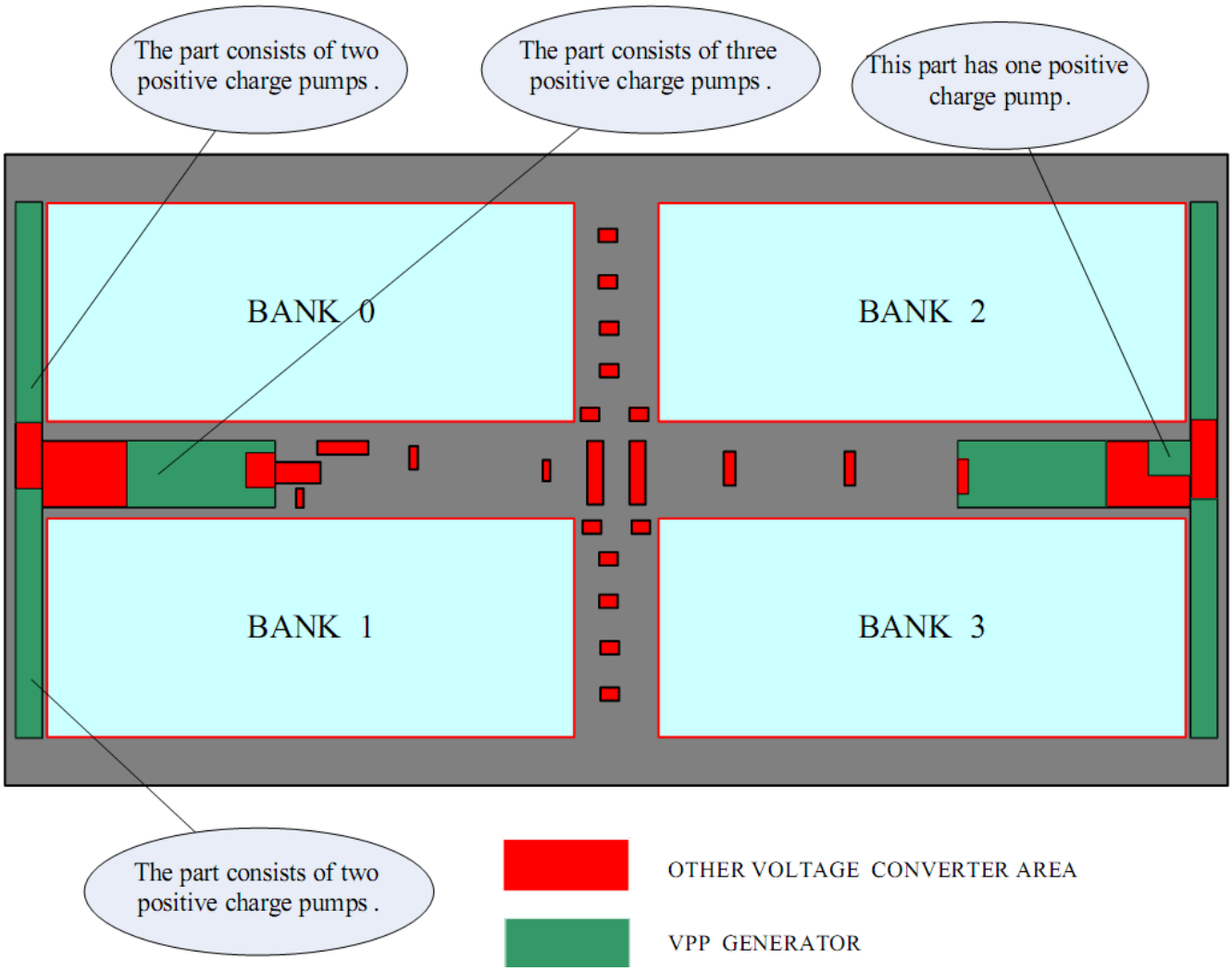
Photograph 4.3.5 Column Redundancy Bitmap

4.4 Location of each internal power

The location of each internal power is illustrated in this section. Almost all the internal powers are generated by charge pumps or power amps, so the location and amount are indicated in each picture.

4.4.1 VPP

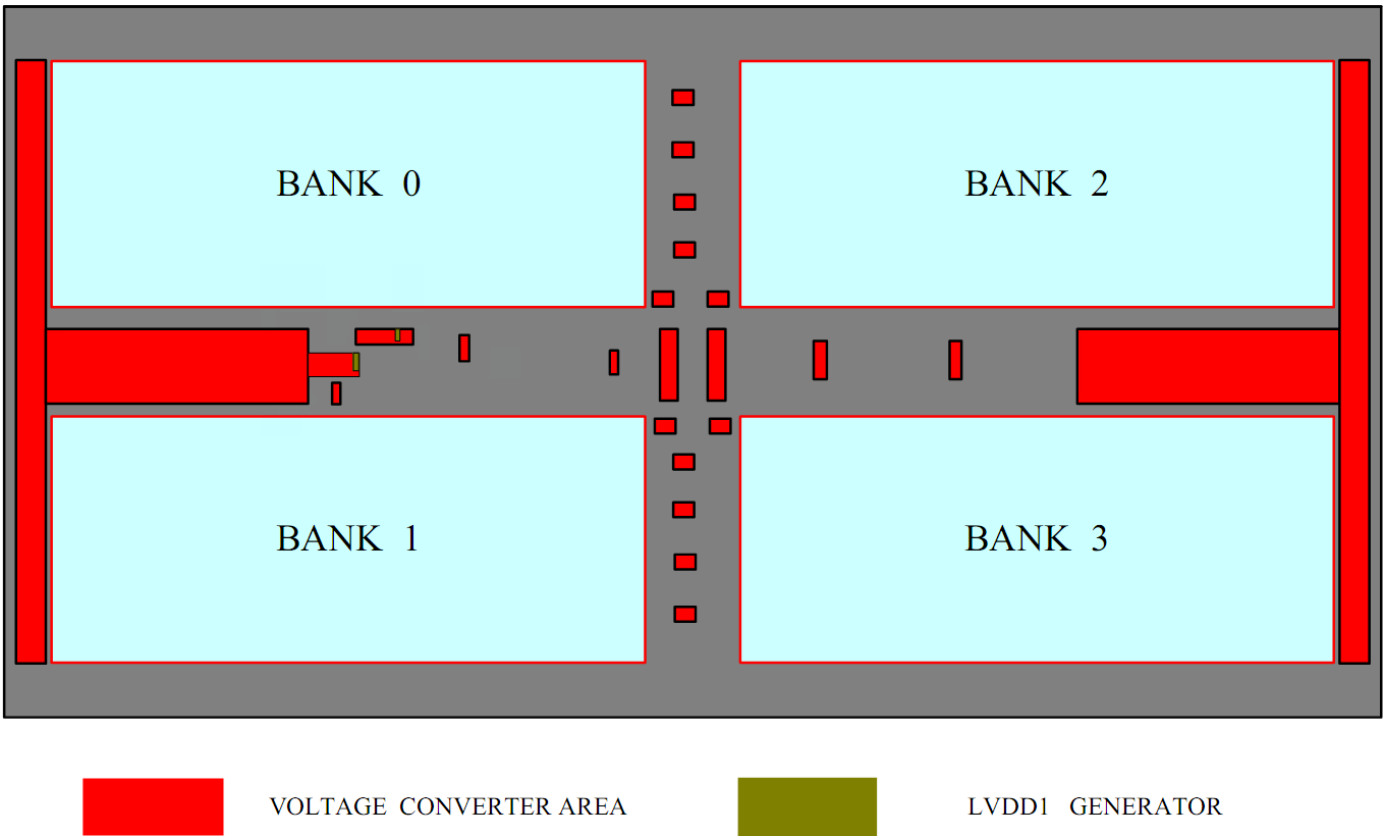
VPP is the supply voltage of Sense Amplify, and the level of the bn of the PMOS used in Sense Amplifier. VPP is generated by 16 charge pumps. The photograph 4.4.1 shows the distribution of the VPP area, and the tips give the number of the sub_area. Through the amount of the charge pumps, we can see VPP is very important voltage for the circuit. Its location shows below:



Photograph 4.4.1 VPP area

4.4.2 LVDD1

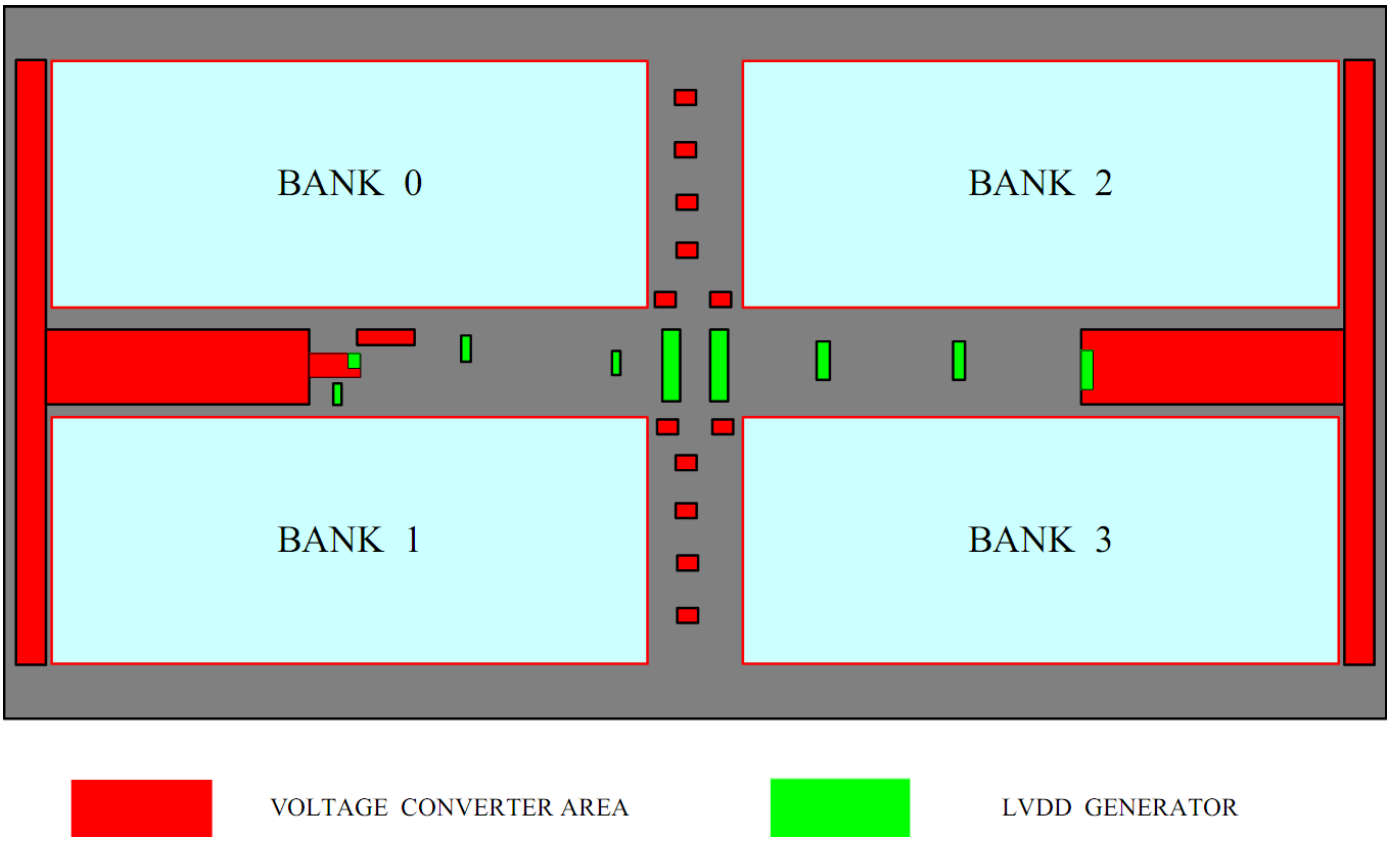
LVDD1 is the power of TEST_OSC. This voltage is from amp's outputs. This regulator's area is small. The location of LVDD1 generator is shown in Photograph 4.4.2.



Photograph 4.4.2 LVDD1 area

4.4.3 LVDD

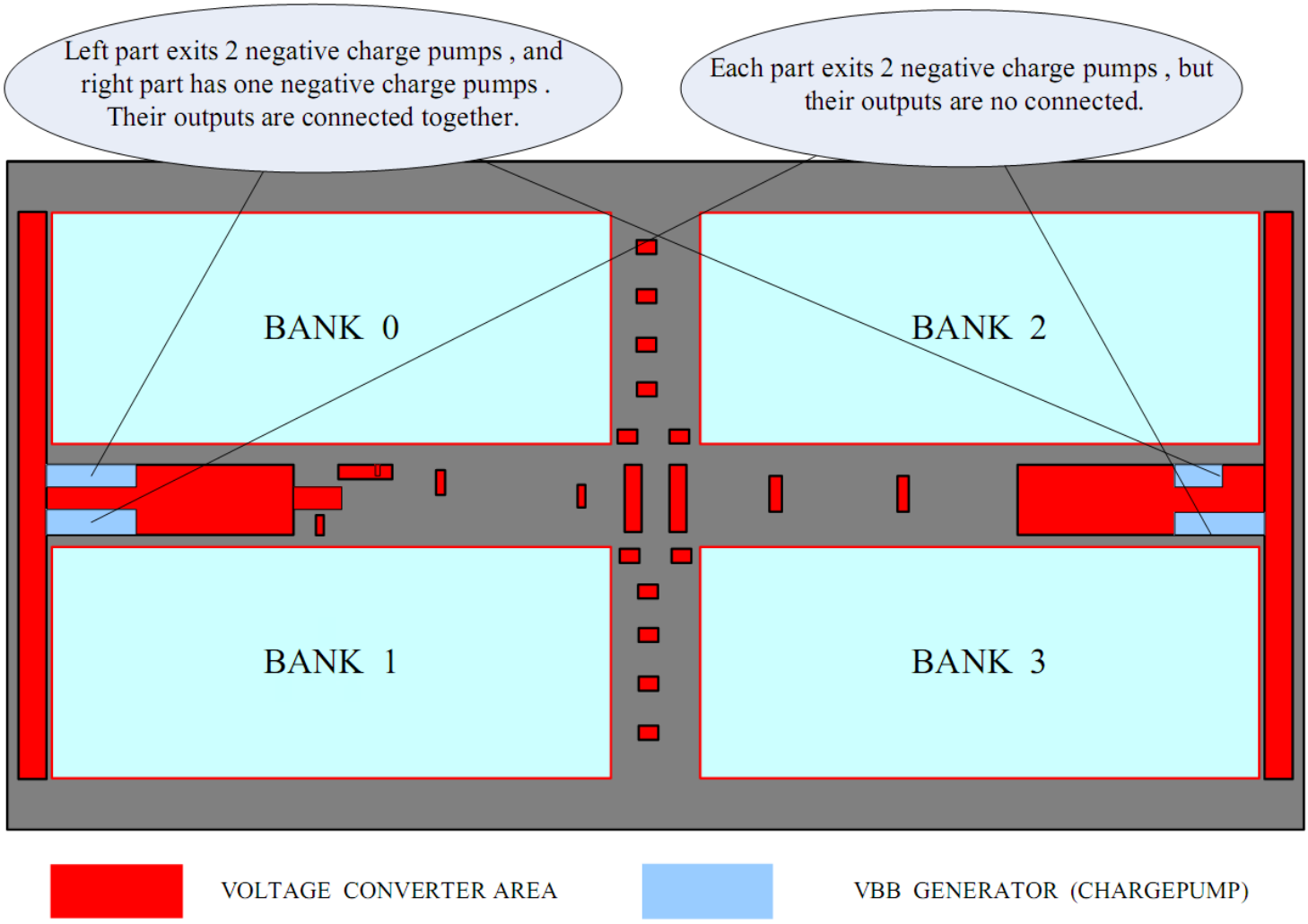
LVDD power is used widely in the chip. It supplies for data path circuit except for DQ Input Buffer and DQ Output, and other circuits like COMMAND Logic, Test MODE, ADDRESS PATH, and so on. LVDD is generated from many power amplifiers. And these power amplifiers' input and output are the same. Also they work at the same time. The detail location is presented in Photograph 4.4.3.



Photograph 4.4.3 LVDD area

4.4.4 VBB

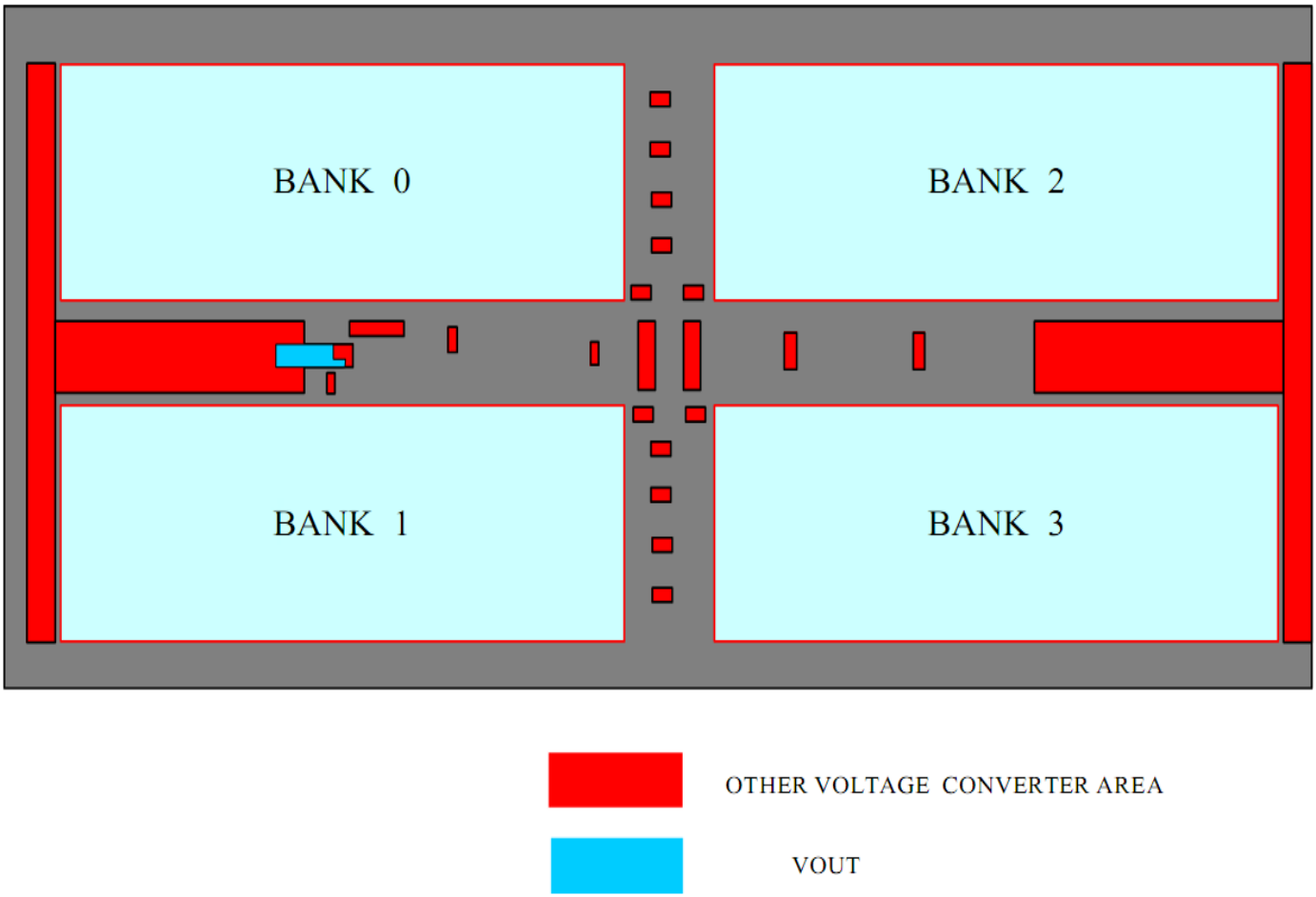
VBB is the substrate of memory cell MOSFET. It's generated by 7 negative voltage charge pumps. They are located in left and right part of this chip. The distribution of all VBB charge pumps is shown in Photograph 4.4.4.



Photograph 4.4.4 VBB area

4.4.5 VOUT

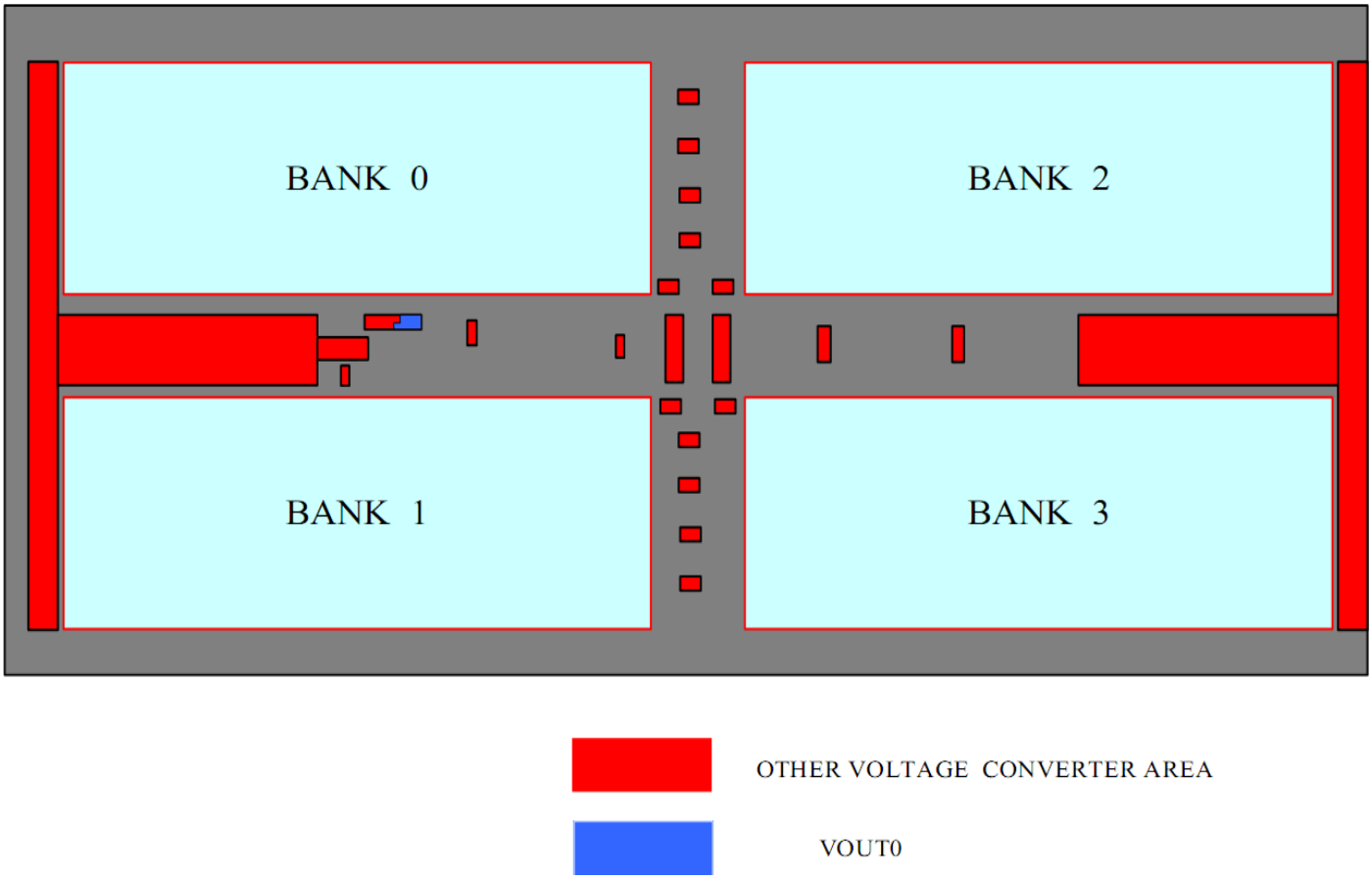
VOUT is reference voltage. The Photograph 4.4.5 shows the location of VOUT.



Photograph 4.4.5 VOUT area

4.4.6 VOUT0

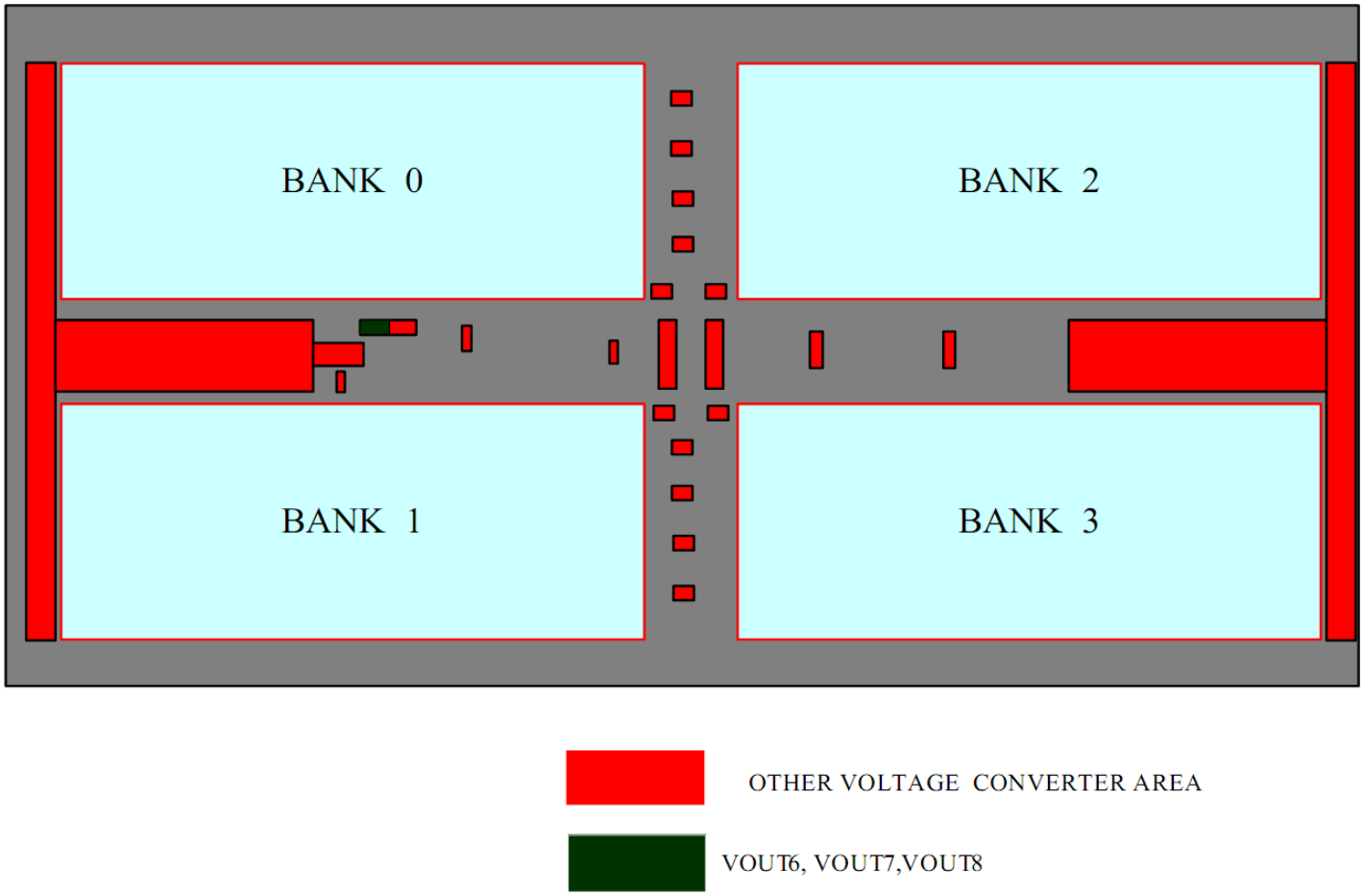
The location of VOUT0 is shown in Photograph 4.4.6.



Photograph 4.4.6 VOUT0 area

4.4.7 VOUT6, VOUT7 & VOUT8

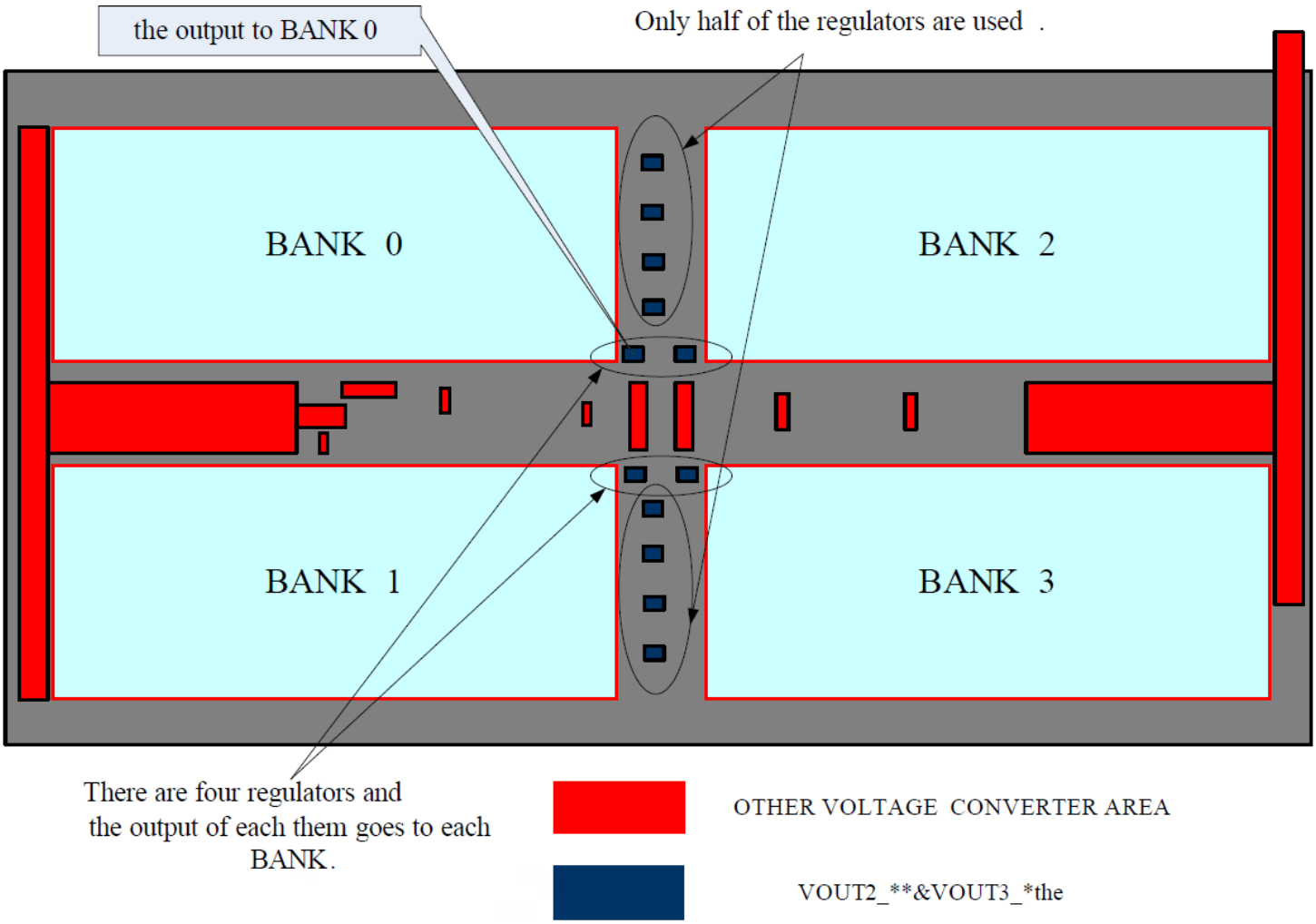
The distribution of VOUT6, VOUT7 and VOUT8 is shown in Photograph 4.4.7.



Photograph 4.4.7 VOUT6, VOUT7 & VOUT8 area

4.4.8 VOUT2_1, VOUT2_2 & VOUT3_1, VOUT3_2, VOUT3_3 and VOUT3_4

The location of these powers is shown in Photograph 4.4.8 .



Photograph 4.4.8

Note: ** as 1 or 2
* as 1, 2, 3, or 4

PART B

Project Data

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1.0 Address Path

The Manufacturer Part No. has 16 address pins including A0-A13, bank address pins BA0 and BA1. This device uses a x8 configuration so A0 – A13 are used for the row addressing and A0 – A9 are used for column addressing. The bank addresses BA0 and BA1 determine which bank is used to read, write or precharge and it is also used to access the Mode Register and Extended Mode Register.

Address Buffers for all address pins (together with bank address pins) are shown in Figure 1.1. Next buffered address AB[13:0] is latched in the address input register (Figure 1.6) and buffered bank address BAB[1:0] is latched in the circuits shown in Figure 1.5. The Address Input Multiplexer (Figure 1.4) and Bank Address Multiplexer (Figure 1.3) are used in test mode.

Column Address Path:

The column address signals are latched in successive registers and reach the output stage dependant on the selectable Additive and CAS latency. The Column address latch with Additive and CAS latency are presented in Figure 1.7 and Figure 1.8. Latched Column Address bit 0 and 1 (AYLA_0, AYLB_0, AYLA_1 and AYLB_1) are used in the datapath control of the sequence of burst data.

The Column Address Path for one Bank is presented in Figure 1.10.

The column redundant circuitry of the chip provides 24 redundant Y access signals for every 1024 normal Y access signals.

Row Address Path:

The Address from address input register ~AR[13:0] is multiplexed (Figure 1.12) with the address from the Refresh Counter (Figure 1.11).

The Row Address Path for one Bank is presented in Figure 1.15. Row address bits 0 to 13 are used to address the Main Wordlines.

The row redundant circuitry provides 232 redundant WL for every 8192 normal WL.

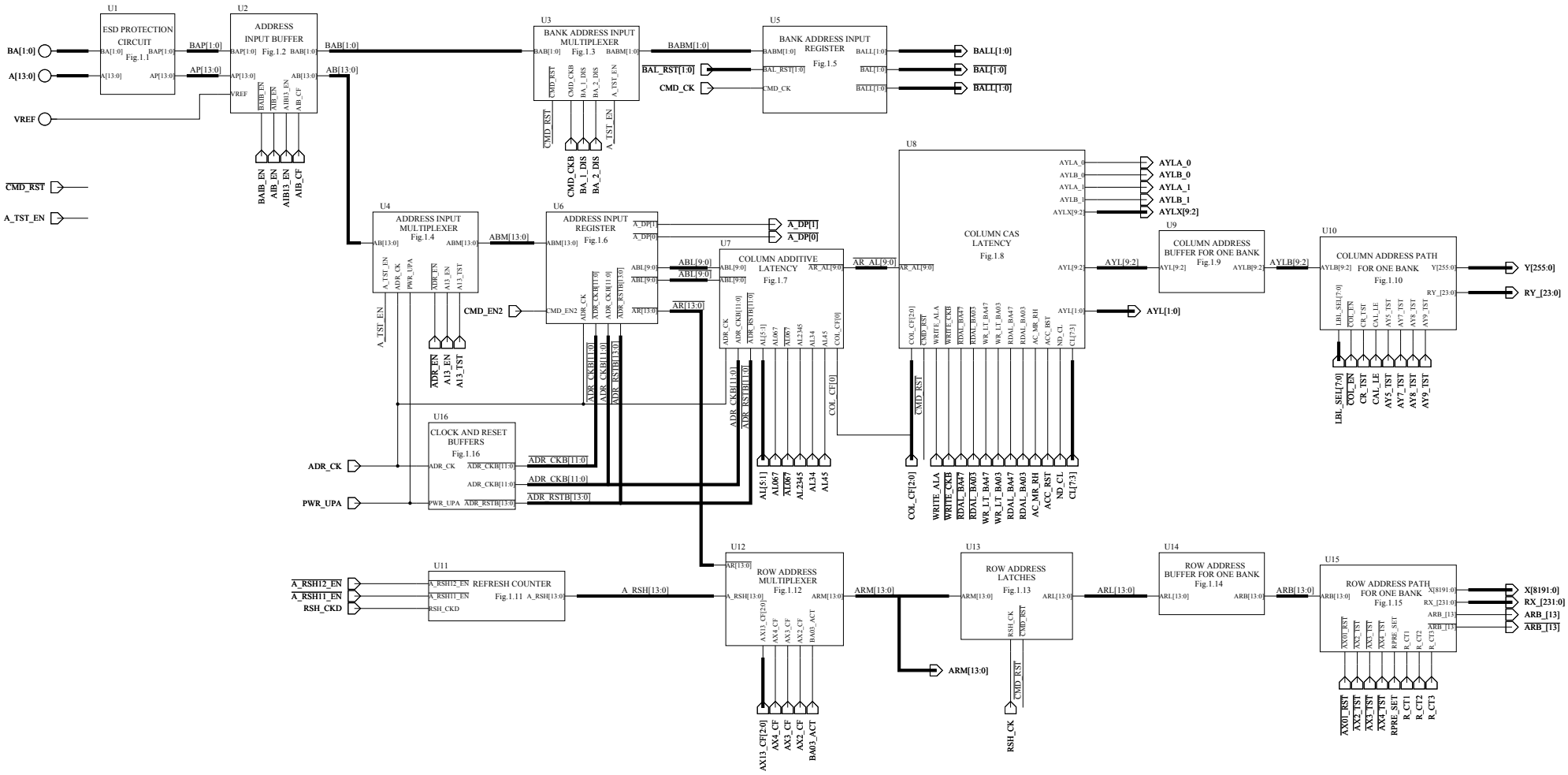

Figure 1.0 ADDRESS PATH

Part No:	
SV No:	Device Type:
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2.0 Data Output Path

This chapter contains information about the data flow from the memory cells to the data pin for the x8 organized Manufacturer Part No.

The block diagram of the read data path is shown in Figure 2.0.

The read path starts with the amplifier data in the BL Sense Amplifiers (Figure 2.1) and next it transfers four bits (for one pin) from the selected bitline LDLs to LDB through the LDL Access. (Figure 2.2). The Local Data Path for Read and Write is presented for one Bank in Figure 2.3. In Figure 2.4 (Data Read Multiplexer) the four bits for each data are multiplexed depending on the device organization and which bank is chosen. The Global Read Data (GDLRA, GDLRB, GDLRC and GDLRD) is driven (Figure 2.5) and saved in the Data Latches Block (Figure 2.6). Circuits in Figure 2.7 provide the first stage serializer of the read data where the four lines for each DQ pin (DRD_A, DRD_B, DRD_C and DRD_D) are converted into two lines (DOUT02 and DOUT13) in series on each line. Figure 2.8 shows the second stage serializer. The data is finally driven onto the pin using the output driver in Figure 2.9. The size of pull up and pull down transistors can be adjusted by the control buses (OBPU_CT[6:0] and OBPD_CT[6:0]) that enable additional transistors in parallel.

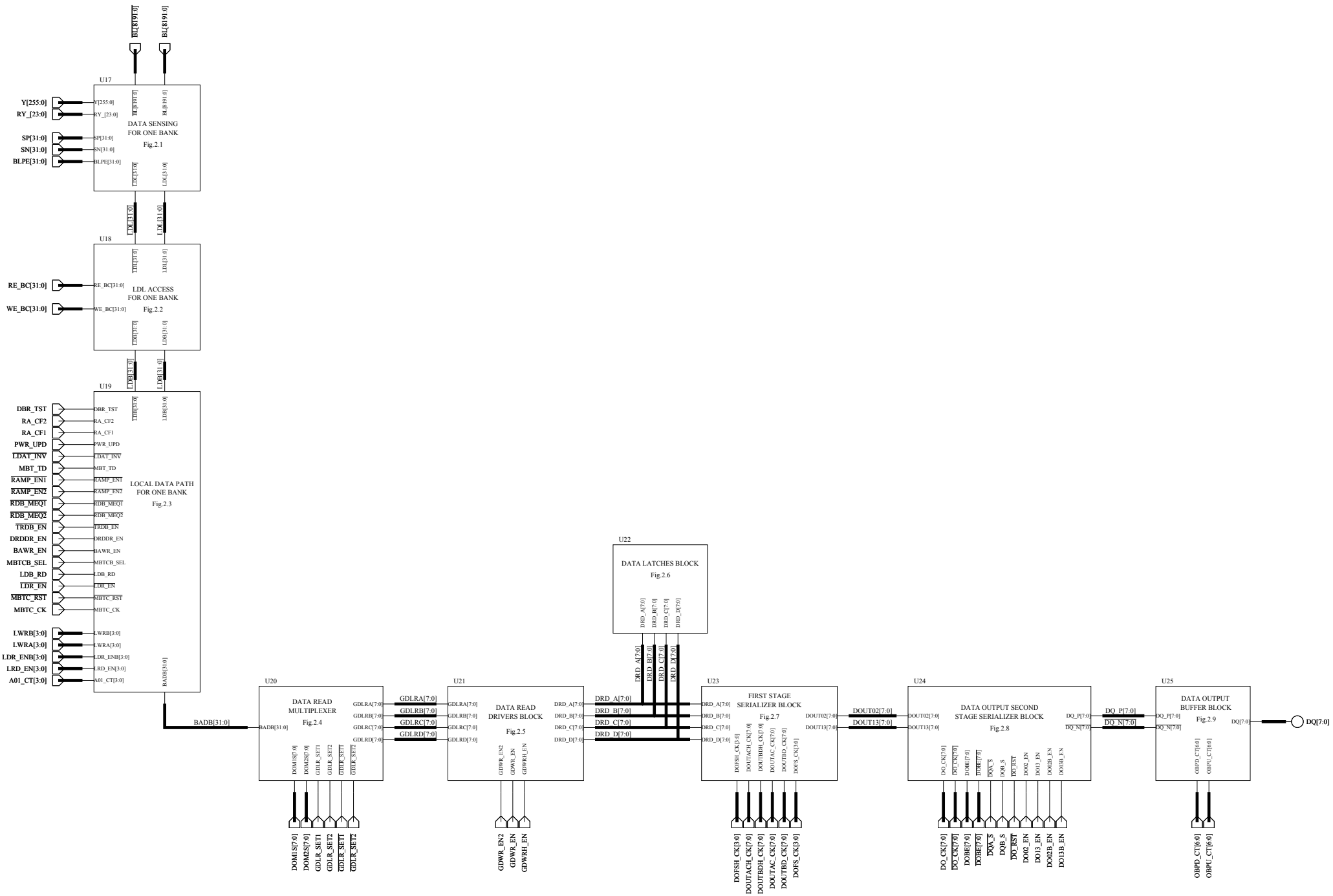

Figure 2.0 DATA OUTPUT PATH

Part No:	
SV No:	Device Type:
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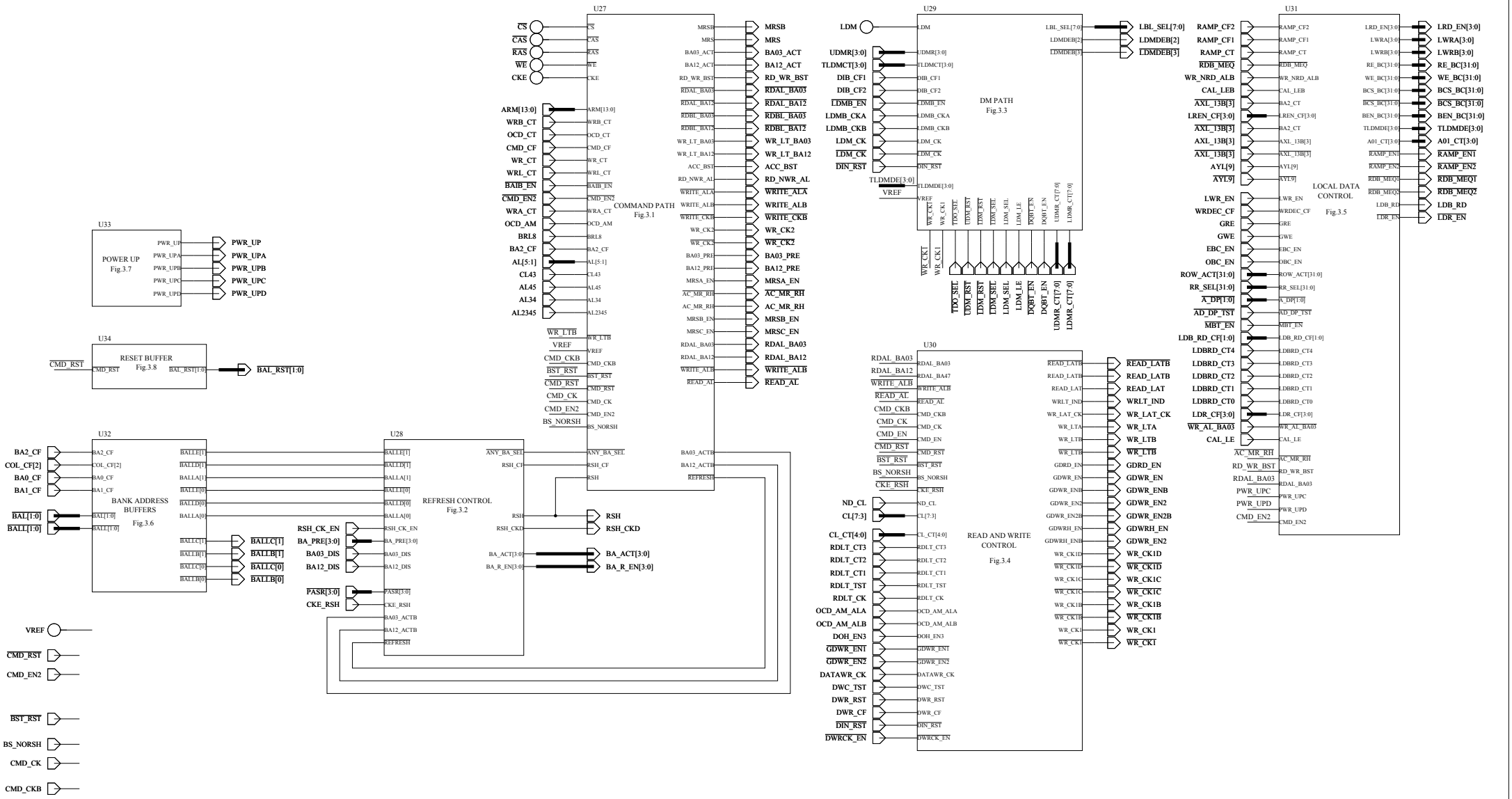
3.0 Control Path

This chapter contains information about the partial control circuitry analyzed on the Manufacturer Part No.

The main blocks in this chapter are:

- Command Path (Figure 3.1)
- Refresh Control (Figure 3.2)
- Data Mask Path (Figure 3.3)
- Read and Write Control (Figure 3.4)
- Local Data Control (Figure 3.5)



Part No:

SV No: Device Type:

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Figure 3.0 CONTROL PATH

PART B

Standard Cells

Appendix

Signal Descriptions →

Signal Name	Description
A[13:0]	Addres Pins
_A_DP[0]	Address bit 0 for Data Path control
_A_DP[1:0]	Addess 0 and 1 for Data, Bits 1 to 0
_A_DP[1]	Address bit 1 for Data Path control
_A_DP[11]	Address bit 11 for Data Path control
A_RSH[12:0]	Address from Refresh Counter, Bits 13 to 0
_A_RSH11_EN	Address bit 11 from Refresh Counter enable signal, Active Low
_A_RSH12_EN	Address bit 12 from Refresh Counter enable signal, Active Low
A_TST_EN	Address Test Enbale signal
A01_CT[3:0]	Address 0 and 1 Data Control, Bits 3 to 0
A13_EN	Address bir 13 Enable signal
A13_TST	Address bit 13 Test signa
AB[13:0]	Address Buffered, Bits 13 to 0
ABL[11:0]	Address Buffered and Latched Bus, Active Low
_ABL[11:0]	Address Buffered and Latched Bus, Active Low
AC_MR_RH	Access, MRS and Refrsesh Command
ACC_BST	Access with Burst
ADR_CK	Address Clock
ADR_CKB	Address Clock
ADR_CKB[11:0]	Address Clock, Bits 11 to 0
_ADR_CKB[11:0]	Address Clock, Bits 11 to 0, Active Low
_ADR_EN	Address Enable signal, active LOW
_ADR_RSTB[13:0]	Address Reset, active LOW, Bits 13 to 0
AIB_CF	Address Input Buffer configuration signal
_AIB_EN	Address Input Buffer enable signal, active LOW
AL[5:1]	Additive Latency, Bits 5 to 1
AL067	Additive Latency 0, 6, 7
AL2345	Additive Latency 2, 3, 4, 5
AL34	Additive Latency 3, 4
AL45	Additive Latency 4, 5
_ANY_BA_SEL	Any Bank Select signal, active LOW
AP[13:0]	Input Address after Protection, Bits 13 to 0
AP_T[3:0]	Test Address, Bits 3 to 0
AR_AL[11:0]	Row Address with Additive Latency, Bits 11 to 0
ARM02_[13:0]	Multiplexed Row Address for Banks 0 and 2, Bits from 13 to 0
ARM13_[13:0]	Multiplexed Row Address for Banks 1 and 3, Bits from 13 to 0
AX01_RST	Row Address bits 0 and 1, reset signal
AX11_9_TST	Row Address bits 9, 10 and 11 test signal
AX5_TST	Row Address bit 5 test signal
AX6_TST	Row Address bit 6 test signal
AX7_TST	Row Address bit 7 test signal
AX8_TST	Row Address bit 8 test signal
AX9_TST	Row Address bit 9 test signal
AX12_TST	Row Address bit 12 test signal
AX13_TST	Row Address bit 13 test signal
AX2_CF	Row Address bit 2 Configuration signal
AX3_CF	Row Address bit 3 Configuration signal
AX4_CF	Row Address bit 4 Configuration signal
AYLB[9:2]	Column Address Buffered, Bits 9 to 2

Signal Name	Description
AYL[9:2]	Column Address Latched, Bits 9 to 2
BA[1:0]	Bank Address Pins
BA_ACT[3:0]	Bank Active, Bits 3 to 0
BA_LT[2]	Bank Address with Latency, Bit 2
BA_PRE[3:0]	Bank Precharge, Bits 3 to 0
BA_R_EN[3:0]	Bank Row Enable, Bits 3 to
BA0_CF	Bank Address bit 0 Configuration signal
BA1_CF	Bank Address bit 1 Configuration signal
BA2_CF	Bank Address bit 2 Configuration signal
BA3_CF	Bank Address bit 3 Configuration signal
BA03_ACT	Bank 0 and 3 Active Command
BA012_ACT	Bank 1 and 2 Active Command
BA47_DIS	Bank Address Disable signal
_BAL_RST[2:0]	Bank Address Reset signal, active LOW
BS_NORSH	Bank Selected and No Refresh
BRL4	Burst Length 4
_BST_RST	Burst Reset signal, active LOW
CAL_LE	Column Latch Enable signal
CAS_ALA	CAS with Additive Latency
CAS_ALB	CAS with Additive Latency
CKE_RSH	CKE or Refresh Command
CL[7:3]	CAS Latency, Bits 7 to 3
CL_CT[4:0]	Column Control, Bits 4 to 0
CL43	Cas Latency 4 or 3
CMD_CF	Command Configuration
CMD_CK	Command Clock
CMD_CKB	Command Clock Buffered
CMD_EN	Command Enable
_CMD_RST	Command Reset signal, active LOW
COL_CF[2:0]	Column Configuration, Bits 2 to 0
_COL_EN	Column Enable signal, active LOW
CR_TST	Column Redundant Test signa
CS_ALA	CS with Additive Latency
DATAWR_CK	Data Write Clock
DBR_TST	Data Bus Read Driver Test signal
DIB_CF	Data Input Buffer Configuration signal
_DIB_EN	Data Input Buffer Enable signal, active LOW
DIN_CKA	Data Input Clock
_DIN_RST	Data Input Reset signal, active LOW
DO_CK[15:0]	Data Output Clock, Bits 15 to 0
_DO_RST	Data Output reset, active LOW
DO02_EN	Data time 0 and 2 Output Enable signal
DO13_EN	Data time 1 and 3 Output Enable signal
DOBE[15:0]	Data Output Buffer Enable
DOFS_CK[3:0]	Data Output First Serializer Clock, Bits 3 to 0
DOUTAC_CK[7:0]	Data Output A or C First Serializer Clock, Bits 7 to 0
DQ[7:0]	Data Pin, Bits 7 to 0
_DQA_S	Data Output Select signal
DQBT_EN	Data Buffer for Test Enable signal

Signal Name	Description
DWC_TST	Data Write Clock Test signal
_DWRCK_EN	Data Write Clock Enable signal, active LOW
GDRD_EN	Global Data Line Read Enable Signal
LBL_CE[7:0]	Column Enable Bus for Logical Blocks, Bits 7 to 0
LBL_SEL[7:0]	Logical Block Select Bus, Bits 7 to 0
LD_INV	Local Data Inversion signal
LDRD_EN	Local Data Read Enable
LRD_EN[3:0]	Local Read Enable signal, Bits 3 to 0
LWR_EN	Local Write Enable
MBT_EN	Multibit Test Enable, active LOW
MBTC_CK	Multibit Comparator Clock
_MBTC_RST	Multibit Comparator Reset, Active LOW
OBPD_CT[6:0]	Output Buffer NMOS Transistor Control, Bits 6 to 0
OCD_AM	On Chip Driver Adjust Mode
OCD_AM_ALA	OCD ADjust Mode, AL Applied
OCD_CT	OCD Program Control signal
PWR_UP	Power Up
R_CT	Row Path Control signal
_R_RST	Row Reset signal, active LOW
RAS_ALA	RAS with Additive Latency
RD_NWR_AL	Read or No Write With Additive Latency
RD_WR_BST	Read or Write with Burst
RDAL_BA03	Read Commnad with Additive Latency for Bank 0 and 3
RDAL_BA12	Read Commnad with Additive Latency for Bank 1 and 2
RDLT_CK	Read Latency Clock
RDLT_IND	Raed Latency Indicator
READ_AL	READ Command with Additive Latency
READ_LAT	Read Command with Latency
_REFRESH	Refresh Command, active LOW
ROW_ACT	Row Active
ROW_RST	Row Reset signal
RPRE_EN	Row Predecoder Enable signal
RPRE_RST	Row Predecoder Reset signal
_RR_ACT	Row Redundant Active signal, active LOW
RR_CT	Row Redundant Control signal
RR_SEL	Row Redundant Select signal
RSH_CF	Refresh Configuration
RSH_CK	Refresh Clock
RSH_CK_EN	Refresh Clock Enable
RSH_CKD	Refresh Clock Delayed
RY_[23:0]	Redundant Y Access
TR3A[12]	Mode Register bit 12 reset signal
VDDI2	VDD Internal Voltage 2
WE_ALA	WE with Additive Latency
WR_CK	Write Clock
WR_CT	Write Control signal
WR_LAT_CK	Write Clock With Latency
WR_LTA	Write Command With Latency
WR_NRD_ALA	Write or No Read With Additive Latency

Signal Name	Description
WR_RD_BST	Write and Read Command with Burst
WRITE_ALA	Write Command With Additive Latency
WRITE_CK	Write Command Clock
WRL_CT	Write Latency Control
WRLT_IND	Write Latency Indicator
XBL_EN	Row Block Enable signal, active LOW
Y[255:0]	Y Access

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