

# FUNCTION ANALYSIS REPORT

**OMAP5432**

— Application Processor



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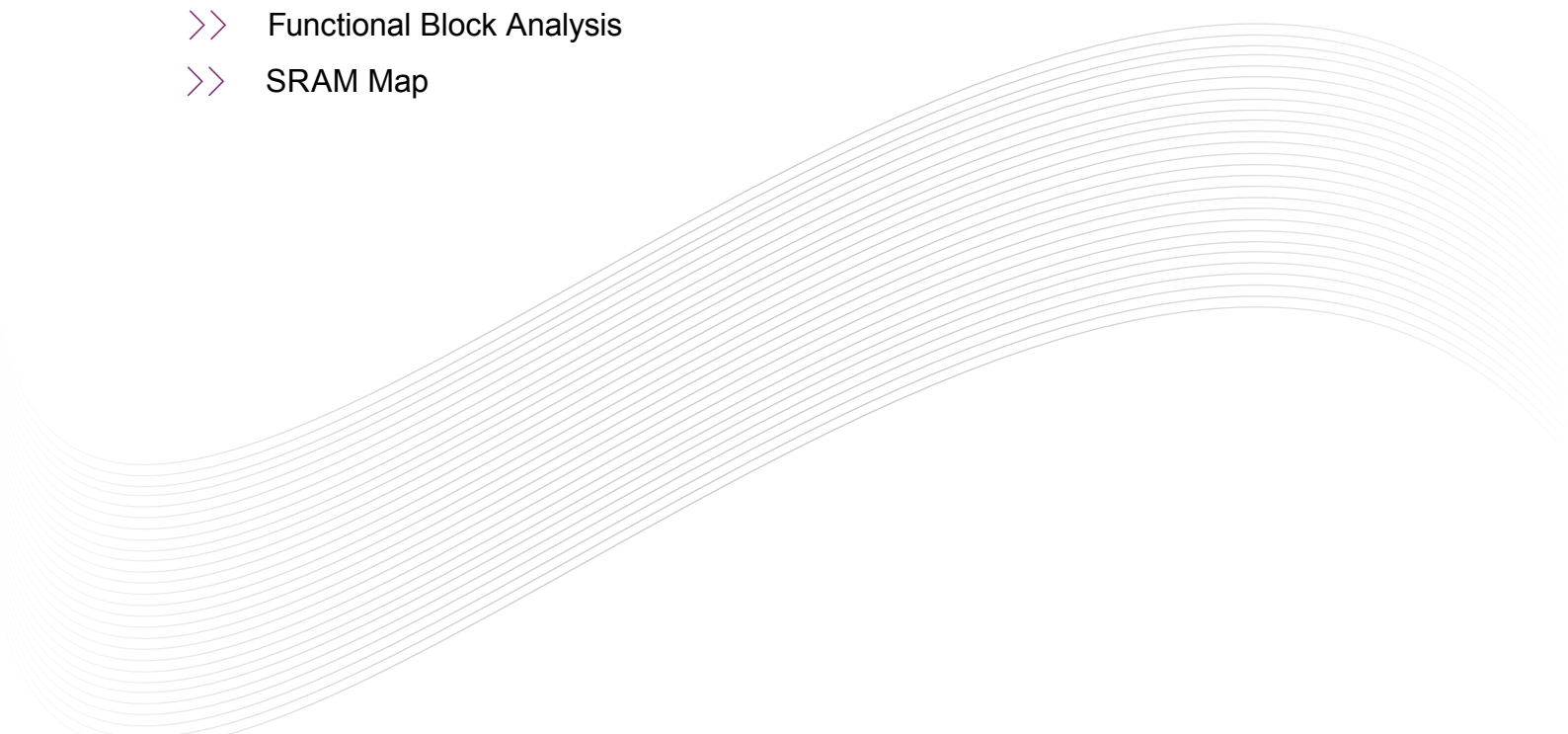


**Part No.** OMAP5432

**Date** 2013-07-25

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Chapter **1**

**PROJECT OVERVIEW**



## 1. Project Overview

### 1.1 Chip Introduction

OMAP™ 5 processors are designed to support high performance applications within a low power envelope, preventing the need for fans.

**Feature:**

- Multicore ARM® Cortex™ processors
- Two ARM Cortex-A15 MPCore processors capable of speeds up to 1.7 GHz
- Two ARM Cortex-M4 processors for low-power offload and real-time responsiveness
- Multi-core POWERVR™ SGX544-MPx graphics accelerators
- Dedicated TI 2D BitBlit graphics accelerator
- IVA-HD hardware accelerators enable full HD, multi-standard video encode/decode as well as stereoscopic 3D (S3D)
- Faster, higher-quality image and video capture

**Application:**

- Mobile computing devices and consumer products

## 1.2 Device Summary

Item	Content
Part Number / Project Number	OMAP5432 / 1130601
Manufacture	TI
Device Type	Processor
Package Marking	TI; X5432AAAN; 32ZCN09; \$N; G1
Package Type	17mm × 17mm BGA, 754 Ball
Die Marking	
Die Size	9.1 mm × 8.8 mm = 80.08mm <sup>2</sup>
Number of Metal Layers	9
Number of Poly Layers	1
Process Type	CMOS
Interconnect Level (Width/Pitch(um))	
Process Generation	28 nm
Feature Measure to Determine Process Generation	Gate Length
Transistor Gate Length	28 nm

Chapter 2

DEVICE IDENTIFICATION



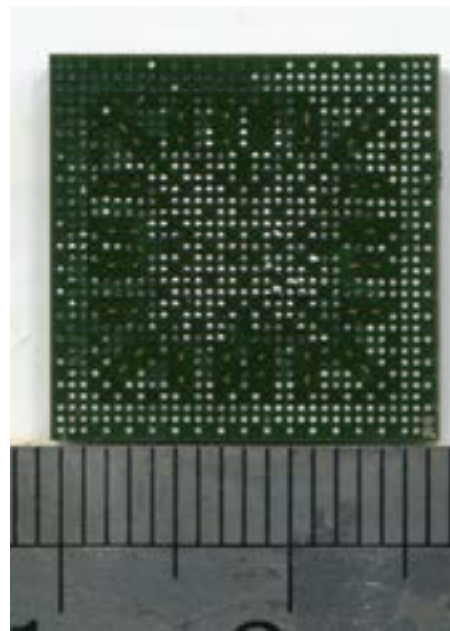


## 2. DEVICE IDENTIFICATION

### 2.1 Package Photo



Top View



Bottom View

Figure 2.1 Package Photo

## 2.2 Die Marking

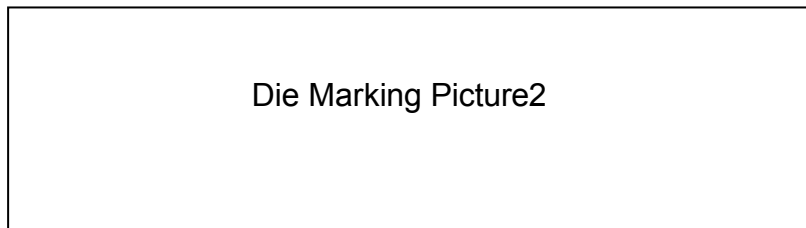


Figure 2.2 Die Markings

## 2.3 Die Photo

Figure 2.3.1 Poly Image

## 2.4 Minimum Pitch of Pads

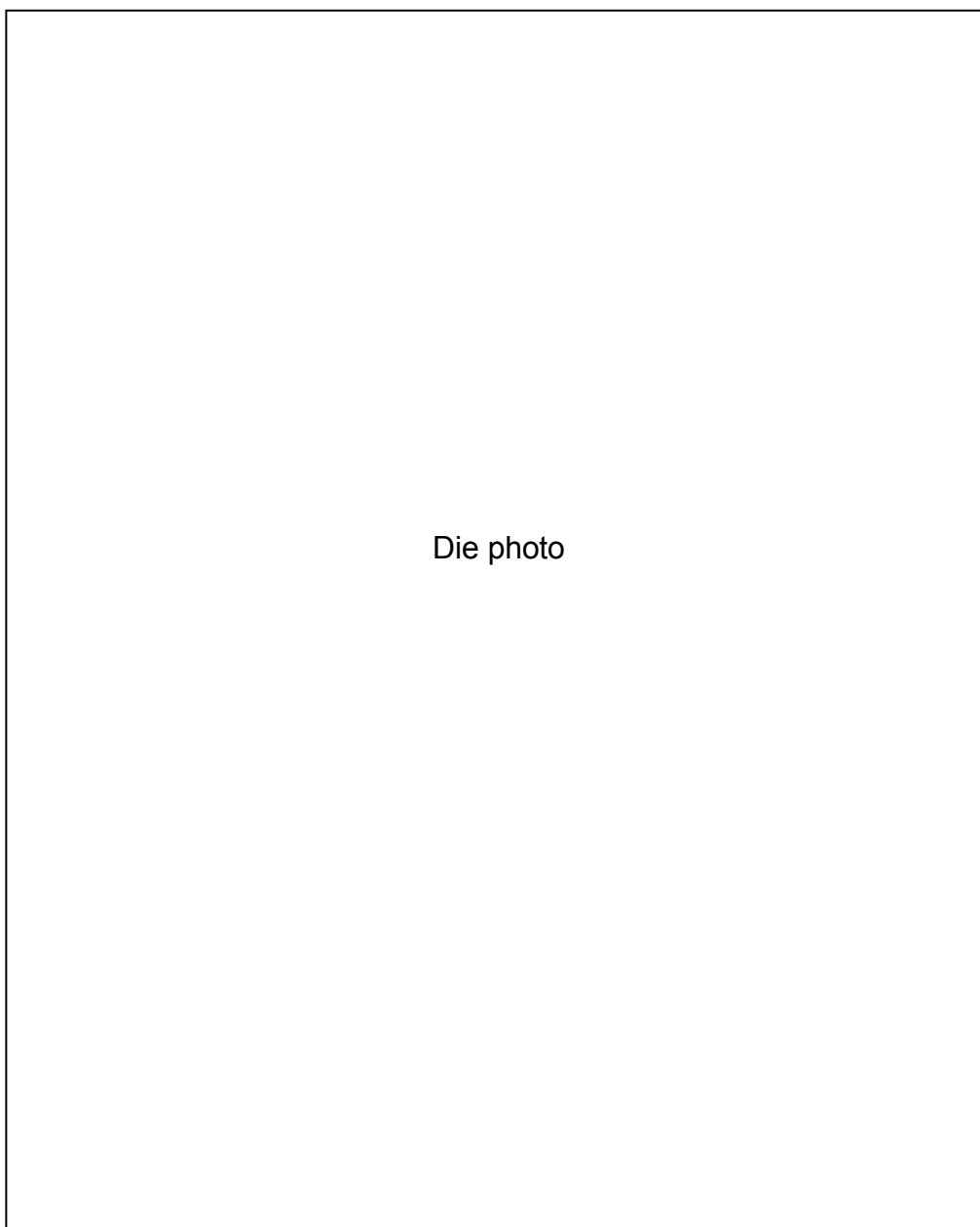


Figure 2.4 Minimum Pitch of Pads

Chapter 3

PROCESS ANALYSIS



### 3. Process Analysis

#### 3.1 General Layers Structure

Figure 3.1 General Layers Structure

### 3.2 Metal Layers Minimum Width and Pitch

Item	Content
Metal 1 Minimum Width	
Metal 1 Minimum Pitch	
Metal 2 Minimum Width	
Metal 2 Minimum Pitch	
Metal 3 Minimum Width	
Metal 3 Minimum Pitch	
Metal 4 Minimum Width	
Metal 4 Minimum Pitch	
Metal 5 Minimum Width	
Metal 5 Minimum Pitch	
Metal 6 Minimum Width	
Metal 6 Minimum Pitch	
Metal 7 Minimum Width	
Metal 7 Minimum Pitch	
Metal 8 Minimum Width	
Metal 8 Minimum Pitch	
Metal 9 Minimum Width	
Metal 9 Minimum Pitch	

### 3.3 Minimum Contacted Pitch and Gate Length Transistor

Item	Content
Minimum Contacted Pitch	62 nm
Gate Length Transistor	28 nm

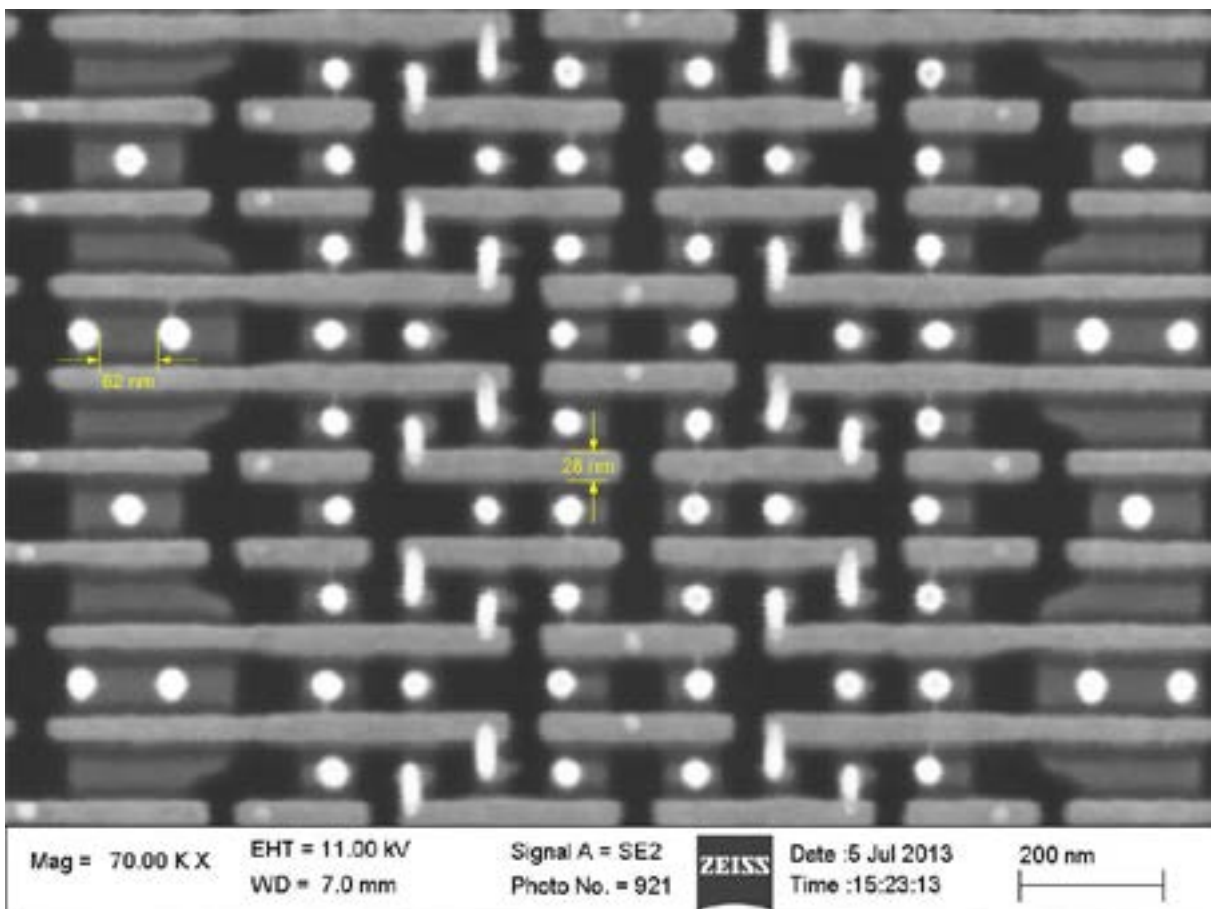


Figure 3.2 Minimum Contacted Pitch and Gate Length Transistor



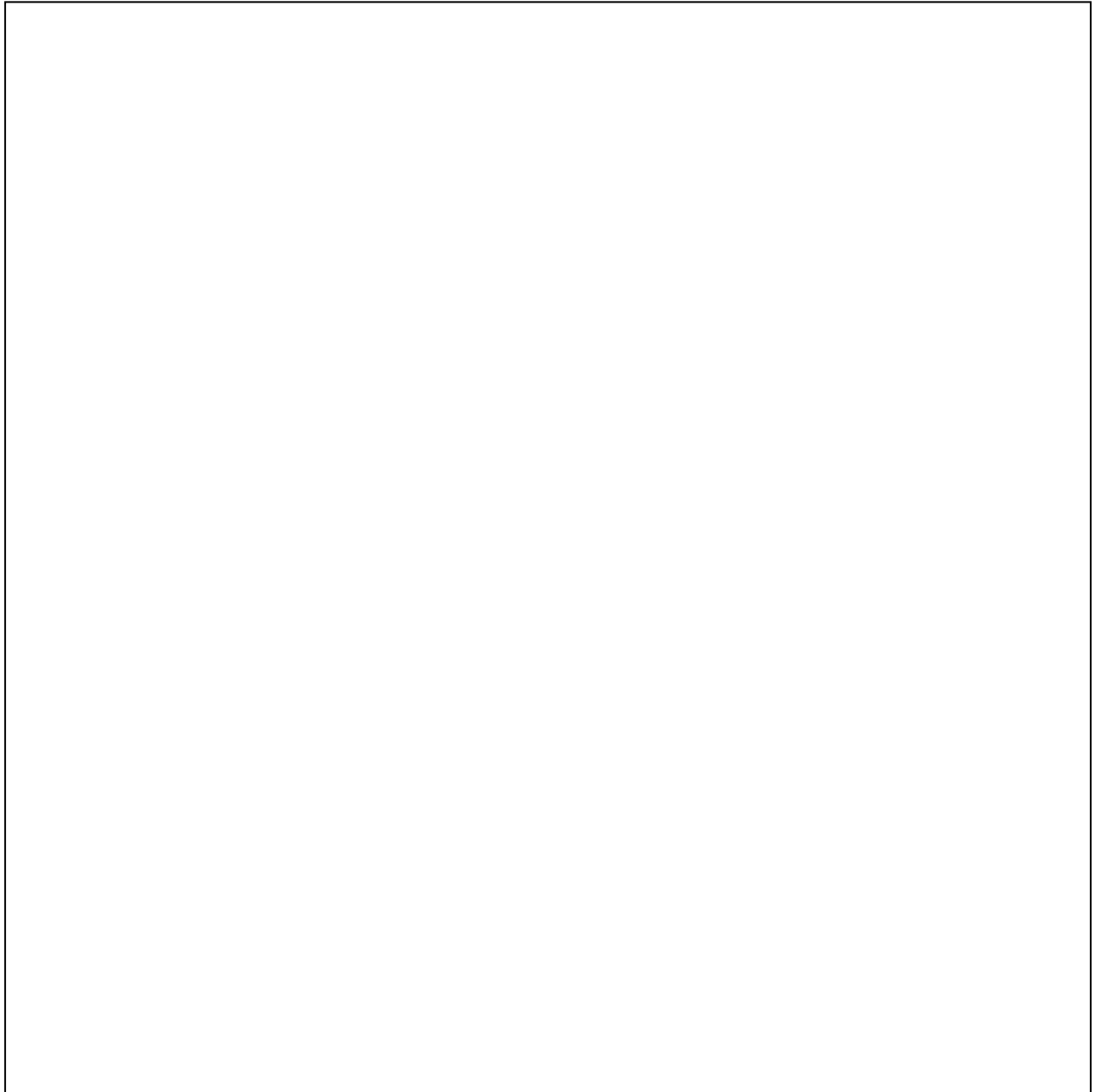
Chapter 4

**FUNCTIONAL BLOCK ANALYSIS**



## 4. Functional Block Analysis

### 4.1 Functional Block Overview



PL Image

Figure 4.1 Functional Block Overview

## 4.2 Functional Block Summary

Item	Content
ARM Cortex-A15 MPCore Size	$X.XX \text{ mm} \times X.XX \text{ mm} = XX.XX\text{mm}^2$
ARM Cortex-M4 Core Size	$X.XX \text{ mm} \times X.XX \text{ mm} = XX.XX\text{mm}^2$

Chapter 5

SRAM MAP



## 5. SRAM Map

### 5.1 SRAM Distribution

Figure 5.1 SRAM Distribution

XXXXXXXXXXXXXXXXXXXXXXXXXXXX  
XXXXXXXXXXXXXXXXXXXXXXXXXXXX

## 5.2 6T SRAM Map

### 5.2.1 6T SRAM Cell Size

Item	Content
6T SRAM Cell Size	

Figure 5.2.1 6T SRAM Cell Size

## 5.2.2 6T SRAM Cell Analysis

Figure 5.2.2 6T SRAM Cell Schematic and Topographical Analysis

## 5.3 8T SRAM Map

### 5.3.1 8T SRAM Cell Size

Item	Content
8T SRAM Cell Size	

Figure 5.3.1 8T SRAM Cell Size



### 5.3.2 8T SRAM Cell Analysis

Figure 5.3.2 8T SRAM Cell Schematic and Topographical Analysis

## 5.4 SRAM Map of L1/L2 Cache

Figure 5.4.1 L1/L2 Cache Distribution of ARM Cortex-A15

XX  
XX.

### 5.4.1 6T/8T SRAM Distribution of L1/L2 Cache

Figure 5.4.1 6T/8T SRAM Distribution of L1/L2 Cache

## 5.4.2 L2 Cache 6T SRAM Unit

### 5.4.2.1 L2 Cache 6T SRAM Unit Size

Figure 5.4.2.1 L2 Cache 6T SRAM Unit Size

### 5.4.2.2 L2 Cache 6T SRAM Unit Capacity

XX  
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX.  
XXXXXXXXXXXXX  
XXXXXXXXXXXXX  
XX

### 5.4.3 L1 Cache 8T SRAM Unit

#### 5.4.3.1 L1 Cache 8T SRAM Unit Size

Figure 5.4.3.1 L1 Cache 8T SRAM Unit Size

### 5.4.3.2 L1 Cache 8T SRAM Unit Capacity

XX  
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX.  
XXXXXXXXXXXXX  
XXXXXXXXXXXXX  
XX

## 5.4.4 L1 Cache 6T SRAM Unit

### 5.4.4.1 L1 Cache 6T SRAM Unit Size

Figure 5.4.4.1 L1 Cache 6T SRAM Unit Size



### 5.4.4.2 L1 Cache 6T SRAM Unit Capacity

XX  
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX.  
XXXXXXXXXXXXX  
XXXXXXXXXXXXX  
XX



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